

RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE

Department of Electronics and Communication Engineering



Certificate Program

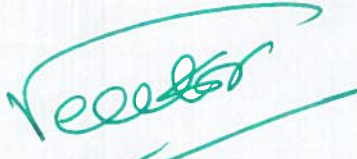
On

“PCB Design ”

Date: 19th to 23th August 2019

Finney Daniel

Director, center for electronics system design
Vijayawada


PRINCIPAL
RISE KRISHNA SAI GANDHI
GROUP OF INSTITUTIONS
VALLURU:: ONGOLE.



RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

(Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada)
NH-16, Valluru, Ongole, Prakasam (District)-523272

Valluru,

Date: 01-08-2019

To

F.Daniel,
Director, Center for Electronics System Design,
Vijayawada.

Dear Sir,

Subject: Inviting for Certificate program - Reg.

Greetings from RISE Krishna Sai Gandhi Group of Institutions, Ongole

As per the discussion with Dr.K.V.Subrahmanyam , Principal, of our Institute, I hereby take this opportunity to invite you to conduct the Certificate program on **PCB Design** " From 19-08-2019 to 23-08-2019.

You are requested to interact and provide guidance to our II B.Tech students, who are looking forward to their bright career ahead. I will feel honored by your gracious presence at our organization. I believe that your lecture will help our students and faculty members to explore knowledge.

Thanking you in anticipation.

Yours sincerely,

Principal

PRINCIPAL

RISE KRISHNA SAI GANDHI
GROUP OF INSTITUTIONS
VALLUR - ONGOLE.

PRINCIPAL

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Finney Daniel

Managing Director

Center for Electronics System Design

Personal Summary

Finney Daniel has a record of organizing Institutional Industry oriented up-gradation programs for undergraduates. Experienced in delivering recent trend technologies to the personnel in vivid methodologies. Providing a lawn of possibilities in the specified area which strengthen the personnel in growing the skills required for their success in the present day competence. He has experience as a guest lecturer, assistant professor and a research fellow. His main interest in this has been to prove the potential and ability of the personnel.

Professional Summary

- Delivered services as Guest Lecturer for VLSI in Andhra University College of Engineering.
- Worked as Assistant Professor in couple of Engineering Colleges.
- As Junior Research Fellow in Defence Research & Development Laboratory.

Areas of Expertise

- **Product Development:** Evolving modules that enable a final product meeting the End- User requirements and facilitate easy utility of the product
- **Project Management:** Maintaining strategic planning and supporting the team in delivering Robust Models by providing employ friendly platform.
- **Organizing Training Sessions:** Planned tabulation for training and hands on expertise for the personnel under training.

Professional Skills and Competencies

- Strong knowledge on Software tools like QUARTUS, Xilinx, Cadence, Tanner- EDA, Mentor- Graphics required for VLSI.
- Good knowledge on hardware design and development includes familiarity in Embedded System tools and PCB design tools like MPLAB Xpress IDE, KEIL, Micro-c, ZUKEN- Cadstar, Eagle, Express-PCB.



PRINCIPAL

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Key Roles

- Academic Director for KR's Educational Society.
- Coordinator for Technical Symposium in Holy Mary Group of Institutions.
- Organized Workshops on Verilog, PCB Design, Prototyping, Embedded Systems, Product Design and Development.


Qualification

- Master of Technology in VLSI-System Design from JNTU-Kakinda.
- PG Diploma in Electronic Product Design from Electronics System Design and Manufacturing (ESDM, Govt. of India).
- Graduation in Electronics & Communication Engineering from CJITS, JNTU- Hyderabad.
- Graduation in Bachelor of Science in Mathematics from Andhra University.

Personal Details

- Born on 21st June 1987 in Visakhapatnam.
- Indian citizen and can speak Hindi, English, Telugu.

Referencs - Available on Request.


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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

PROPOSAL FORM

SUB: Certificate program -Program.

TO THE SECRETARY/CORRESPONDENT THROUGH PRINCIPAL FOR KIND APPROVAL

1	NAME OF THE INSTITUTION	Rise Krishna Sai Gandhi Group of Institutions
2	NAME OF THE DEPARTMENT	Electronics & Communication Engineering
3	TITLE OF THE PROGRAMME	Certificate program
4	NAME OF THE PROGRAMME	Certificate program on “ PCB Design for Electronic Designs”
5	OBJECTIVE OF THE PROGRAMME	To bring the exposure in the PCB Design.
6	DETAILS OF RESOURCE PERSON(S)& CV ATTACHED.	Finney Daniel Director, center for electronics system design Vijayawada.
7	PROPOSED DATE(S)/ACADEMIC YEAR	19-08-2019 to 23-08-2019
8	DURATION OF THE PROGRAMME	FIVE DAY
9	VENUE	Seminar Hall
10	TARGETS	II ECE students
11	No. OF PARTICIPANTS	129 Students
12	REGISTRATION FEE	Free
13	NAME OF PROGRAMME CO ORDINATOR(S)	Mr. K.Nagahanuma Chari
14	NAME OF THE STUDENTS COORDINATOR(S)	1.Mr. Gadde Rajesh (188B1A04A2) 2.Ms.Shaik Shalima (188B1A0435)


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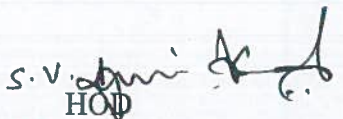
Department of Electronics and Communication Engineering

15	SOURCE OF FUND IDENTIFIED	Management
16	MANAGEMENT CONTRIBUTION REQUIRED	YES
17	PROPOSAL PREPARED BY	Mr.K.Nagahanuma Chari (CO-ORDINATOR)


Coordinator



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S.V. Chari
HOD
HEAD OF THE DEPARTMENT
Department of E.C.E
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P.-523 272



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NH-16, Valluru, Ongole, Prakasam (District)-523272
Department of Electronics and Communication Engineering

Valluru,
Date: 16-08-2019.

CIRCULAR

This is to inform II B.Tech students and faculty that there will be a 5-Day Certificate program on “PCB Design” from 19-08-2019 to 23-08-2019 by F.Daniel, Director, Center for Electronics System Design, Vijayawada.

Copy to:

Principal

Staff Circular

Students of ECE II year

ECE Department Notice Boards

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S.V. Daniel
HOD
HEAD OF THE DEPARTMENT
Department of E.C.E
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P.-523 272



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Department of Electronics and Communication Engineering

Certificate Program on "PCB Design"

Date: 19th to 23rd August 2019

SCHEDULE FROM 19-08-2019 TO 23-08-2019

S. No	Program List	Timing	
		From	To
DAY - 01 (19-08-2019)			
1	Program started	09.00 AM	--
2	Lamp lighting	09.00 AM	09.10 AM
3	Principal speech	09.10 AM	09.25 AM
4	HOD Introduction about PCB Design	09.25 AM	09.35 AM
5	Tea Break	09.35 AM	10.00 AM
6	Introduction about PCB concepts	10.00 AM	01.00 PM
7	Lunch Break	01.00 PM	01.45 PM
8	KI-CAD Software Practical Section	01.45 PM	05.00 PM
DAY - 02 (20-08-2019)			
9	Concepts of PCB Designing, PCB Materials, Layers	09.00 AM	12.15 PM
10	Lunch Break	12.15 PM	01.00 PM
11	Multilayer Concepts	01.00 PM	05.00 PM
DAY - 03 (21-08-2019)			
12	PADSTACK	09.00 AM	12.15 PM
13	Lunch Break	12.15 PM	01.00 PM
14	Schematic entry KI-CAD tools	01.00 PM	05.00 PM
DAY - 04 (22-08-2019)			
15	Drawing a schematic FLAT	09.00 AM	12.15 PM
16	Lunch Break	12.15 PM	01.00 PM
17	BOM. Net list generation	01.00 PM	05.00 PM
DAY - 05 (23-08-2019)			
18	Designing Boards	09.00 AM	12.15 PM
19	Lunch Break	12.15 PM	01.00 PM
20	Drawing a schematic HIERARCHICAL Design	01.00 PM	04.15 PM
21	Certificate Program Exam	04.15 PM	04.45 PM
22	Vote of Thanks	04.45 PM	05.00 PM

M. S. V.
Coordinator

V. S. S.
PRINCIPAL

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RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING
CERTIFICATE PROGRAM FEEDBACK ANALYSIS


A.Y: 2019-2020

Year : II B.Tech ECE


Date: 23-08-2019

Name of the Certificate Program: PCB Design

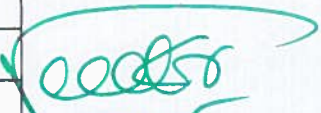
S.No	Roll Number	Name	1	2	3	4	5	6
1	168B1A0452	SRIKANTH	5	4	5	4	5	5
2	188B1A0401	ABOTHU DIVYA	5	4	5	4	5	4
3	188B1A0402	ADIPUDI NAGA LAKSHMI NIKHITHA	4	5	4	5	5	5
4	188B1A0403	ATHYALA JOYSIRIYA	4	4	5	4	4	4
5	188B1A0404	AVVARU ANUSHA	5	5	5	4	4	5
6	188B1A0405	BATTULA RAJANI	4	4	5	4	5	5
7	188B1A0406	BELLAMKONDA SRI VENKATESWARA	4	4	5	4	4	5
8	188B1A0407	CHIMAKURTHI NAGA LAKSHMI PRAVALLIKA	5	4	4	5	5	4
9	188B1A0408	CHALLA SAI LAKSHMI SANTHOSHI	4	4	5	4	4	5
10	188B1A0410	DACHARLA SUPRAJA	4	5	5	4	5	4
11	188B1A0411	DESIREDDY SUMATHI	4	4	4	4	5	5
12	188B1A0412	DIVI SIVANI	4	5	5	4	5	4
13	188B1A0413	GANGIREDDY DHANA LAKSHMI	4	4	5	4	5	5
14	188B1A0414	GOLLA JYOSHNA	4	5	5	4	5	5
15	188B1A0415	JALLI BRIGHTY MANVITHA	4	4	5	5	5	5
16	188B1A0416	JASHTI LAKSHMI DEVI	5	5	4	4	5	4
17	188B1A0417	KAMJULA NAGA ANUHYA	4	5	5	4	5	5


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S.No	Roll Number	Name	1	2	3	4	5	6
18	188B1A0418	KANAMARLAPUDI DIVYA JYOTHI	4	5	4	5	5	4
19	188B1A0419	KAMJULA SUJATHA	4	4	5	5	5	5
20	188B1A0420	KONKIMUDUSU MADHAVI	5	5	5	5	5	5
21	188B1A0421	KOPPOLU SATHVIKA	4	5	4	5	5	5
22	188B1A0422	KOTHURI KOTI SAI SUPRIYA	4	4	5	4	5	4
23	188B1A0423	KOTTURU USHA RANI	4	4	5	4	4	5
24	188B1A0424	KOYI SRI POOJITHA	5	4	4	4	4	5
25	188B1A0425	MAKKENA YASODAMMA	5	5	5	5	5	5
26	188B1A0426	MITTA ANJALI	5	4	5	4	4	5
27	188B1A0427	MOPIDEVI ANUSHA	5	4	5	5	5	4
28	188B1A0428	NALAMALAPU KAVYA	5	5	4	4	4	5
29	188B1A0429	PATAN SHAMA	4	4	5	4	5	5
30	188B1A0430	PATRI NAGA BHAVANA	5	4	5	4	5	4
31	188B1A0431	PERAM SWAPNA	5	4	5	4	5	5
32	188B1A0432	PINNINTI NAVYA	5	5	4	4	4	5
33	188B1A0433	PITTU SAI BHARGAVI	5	5	4	5	4	5
34	188B1A0434	PULAKANAM AKHILA	5	4	4	4	5	4
35	188B1A0435	SHAIK SHALIMA	5	5	4	5	5	5
36	188B1A0436	SHEIK SALMA	5	4	5	4	4	4
37	188B1A0437	THATIKONDA LAVANYA	5	5	5	4	4	5


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S.No	Roll Number	Name	1	2	3	4	5	6
38	188B1A0438	UDALA VENKATA LAKSHMI PRIYA	5	4	5	4	4	5
39	188B1A0439	VANKADARI GAYATRI	4	5	5	4	4	4
40	188B1A0440	YAKKALA VENKATA NIKHILA	5	4	5	4	5	5
41	188B1A0441	YELCHURI LAKSHMI PRASANNA	5	4	4	5	5	5
42	188B1A0442	ATTALURI PAVAN RENUKA CHARI	5	4	5	5	5	5
43	188B1A0443	BEZAWADA SREEKANTH	5	5	5	5	5	4
44	188B1A0444	BOLLA GANGADHAR	5	4	4	4	4	5
45	188B1A0445	ELCHURI VINAY KUMAR	5	5	5	5	5	5
46	188B1A0446	JAGANNADHAM NAVEEN KUMAR	4	5	4	5	4	5
47	188B1A0447	KANAMARLAPUDI SATYAVARDHAN	5	4	4	4	5	5
48	188B1A0448	KARNA PAVAN KUMAR REDDY	5	5	5	5	5	5
49	188B1A0449	KURAPATI VIDYASAGAR	4	4	5	5	4	4
50	188B1A0450	MALLAVARAPU VENKATA RAMI REDDY	5	4	5	4	5	5
51	188B1A0451	MALASANI VENKATA VAMSI KRISHNA	5	4	5	4	5	5
52	188B1A0452	MEDA HARISH	5	4	5	5	5	5
53	188B1A0453	P U V N S M JANAKIRAM SHARMA	5	4	5	4	5	5
54	188B1A0454	RALLAPALLE VEERA VISHNU	5	4	5	4	5	5
55	188B1A0455	SHAIK ABDHUL AZEESH	5	4	5	4	5	5
56	188B1A0456	SHAIK ANIL KUMAR	5	4	4	4	5	5
57	188B1A0457	THOTA GNAN VAMSI SAI KRISHNA	5	5	5	4	5	5



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S.No	Roll Number	Name	1	2	3	4	5	6
58	188B1A0458	THOTA GOPI	5	5	5	5	5	5
59	188B1A0459	VAKA PRAVEEN KUMAR REDDY	5	5	5	4	5	5
60	188B1A0461	ALLU LAKSHMI	5	4	4	4	5	5
61	188B1A0462	BOLLISSETTY JYOTHIRMAY	4	4	5	5	4	4
62	188B1A0463	CHAKKA ANUHYA	5	4	5	4	5	5
63	188B1A0464	CHAKRALA MANIMALA	5	4	5	4	5	5
64	188B1A0465	CHEEDELLA DIVYASRI	5	4	4	4	4	5
65	188B1A0466	CHOUTA VYSHNAVI	5	5	5	5	5	5
66	188B1A0467	DASARI AMRUTHA	4	5	4	5	4	5
67	188B1A0468	DUMPA ANJALI	5	4	4	4	5	5
68	188B1A0469	ENIKAPATI ANITHA	5	4	4	4	5	5
69	188B1A0470	ENIKAPATI ANUSHA	5	5	5	4	5	5
70	188B1A0471	GAJJALA SANDHYA	5	4	5	4	4	5
71	188B1A0472	GARLAPATI KAMALA KUMARI	5	4	5	4	5	4
72	188B1A0473	GOLI SOWMYA	4	5	5	5	4	5
73	188B1A0474	KAMJULA VASANTHA LAKSHMI	5	4	5	4	5	5
74	188B1A0475	KARI SAHITHI	5	5	5	5	4	5
75	188B1A0476	KOPPARTHI HYMAVATHI	5	5	4	5	5	5
76	188B1A0477	KOTA RENUKA	5	5	5	4	5	4
77	188B1A0478	LEBAKA SASI BALA	5	4	5	5	5	4


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S.No	Roll Number	Name	1	2	3	4	5	6
78	188B1A0479	MEDIDA MOUNIKA	5	4	5	4	5	5
79	188B1A0480	MOPIDEVI NAGA NANDINI	5	5	5	4	5	5
80	188B1A0481	MULI BINDU	5	4	4	4	5	5
81	188B1A0482	NARIPEDDI MEGHANA	5	4	5	5	5	4
82	188B1A0484	PATHAN SHYLABANU	4	5	5	4	5	5
83	188B1A0485	PERLA PRAVALLIKA	5	5	5	4	5	5
84	188B1A0486	PINISSETTY RAJITHA	4	5	5	5	5	5
85	188B1A0487	SANDIREDDY SOUNDARYA	5	4	5	5	4	4
86	188B1A0488	SHAIK SHARMILA	4	5	4	4	4	5
87	188B1A0489	SOMINENI JYOTHSNA	5	5	5	5	5	5
88	188B1A0490	TANGA SAI RAMYA	4	4	5	4	4	4
89	188B1A0491	TURIMELLA SRAVANI	5	4	5	5	5	4
90	188B1A0492	VEMURI SHAHINA	5	5	5	4	4	5
91	188B1A0493	YALLATURI DEVI SIRISHA	5	5	5	5	5	5
92	188B1A0494	ANCHULA VENKATESWARLU	4	4	5	5	4	5
93	188B1A0495	B BHARATH KUMAR REDDY	4	5	5	4	5	4
94	188B1A0496	BETHAMSETTY VAMSIKRISHNA SAISR.INIVAS	5	5	4	5	5	5
95	188B1A0497	BODDU JANARDHAN RAO	4	5	5	4	5	5
96	188B1A0498	BUKKA PRABHU TEJA	5	5	5	4	5	5
97	188B1A0499	BURLA PRANEETH REDDY	4	5	5	5	5	5



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S.No	Roll Number	Name	1	2	3	4	5	6
98	188B1A04A0	DAMERLA VAMSI KRISHNA	5	4	5	5	4	4
99	188B1A04A1	DHARMAVARAPU THARUN KUMAR	4	5	4	4	4	5
100	188B1A04A2	GADDE RAJESH	5	4	4	4	5	5
101	188B1A04A3	KARAMSETTY J CH P VENKATA SAI MANEESH	5	4	5	5	5	4
102	188B1A04A4	KOCHARLA KARTHIK	5	5	5	4	4	5
103	188B1A04A5	KOLLIPARA PAVAN KALYAN	5	5	5	5	5	5
104	188B1A04A6	MANDLA SRINIVASULU	4	5	5	5	4	5
105	188B1A04A7	NALLAGUNDLA VINAY KUMAR	4	5	5	4	5	4
106	188B1A04A8	PASUPULETI GOPI KRISHNA	5	4	4	5	5	5
107	188B1A04B0	SEELAM RAMU	4	5	5	4	5	5
108	188B1A04B1	SHAIK HEMANTH BABU	5	5	5	4	5	5
109	188B1A04B2	TANGUTURI KUMAR	4	5	5	5	5	5
110	188B1A04B3	VADITHE SIVA PRASAD NAIK	5	5	5	5	4	4
111	188B1A04B4	VAIDALA GIREESH REDDY	4	5	4	4	4	5
112	188B1A04B5	VELICHERLA PRABHAKAR REDDY	5	5	5	5	5	5
113	188B1A04B6	VUTUKURI BALASURYA PRADEEP	4	4	5	4	4	4
114	188B1A04B7	YADALA BENNI	5	4	5	5	5	4
115	188B1A04B8	KESANA AISHWARYA BHAVANI	5	5	5	4	4	5
116	188B1A04B9	BATTINI VENKATA PRASAD	5	5	5	5	5	5
117	198B5A0401	APPALA SARVANI	4	5	4	4	4	5

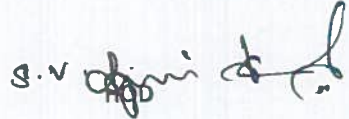

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S.No	Roll Number	Name	1	2	3	4	5	6
118	198B5A0402	BANDLA VENKATA NIKHITHA	5	4	5	5	5	4
119	198B5A0403	PULICHARLA DEEPIKA	4	5	4	4	4	5
120	198B5A0404	VEGURI SWATHI	5	5	5	5	5	5
121	198B5A0405	ANKIREDDY VAMSI	4	4	5	4	4	4
122	198B5A0406	ARLA CHANDRA SHEKHAR	5	4	5	5	5	4
123	198B5A0407	GORREMUCHHU SANDEEP	5	5	5	4	4	5
124	198B5A0408	GUNIMINI SAI	5	5	5	5	5	5
125	198B5A0409	KALLURI SARATH	5	5	5	5	5	5
126	198B5A0410	PULUGU DEVENDAR REDDY	5	5	5	5	5	5
127	198B5A0411	PUNNEPALLI RAKESH	5	5	5	5	5	5
128	198B5A0412	SHAIK AZIS	4	5	4	4	4	5
129	198B5A0413	NARAYANAM SREE VASU	5	4	5	5	5	4
			4.68	4.53	4.74	4.45	4.68	4.75
			93.55	90.61	94.78	89.04	93.57	94.96


Coordinator


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HEAD OF THE DEPARTMENT
Department of E.C.E
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P.-523 272



RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE
DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: *K. Sathvika*
Roll No : *188BIA0421*
Topic : Certificate Program on "PCB Design"

Date: 23-08-2019

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?		✓			
2	Is the certification program well planned or not?	✓				
3	Lecture makes objectives clear?		✓			
4	Lecture speaks clearly and audibly?	✓				
5	Lecture explains with exaples clearly?	✓				
6	Is you are doubts clarified or not?	✓				

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

K. Sathvika
Student Signature

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: *N. Kavya*
Roll No : *188B1A0428*
Topic : Certificate Program on "PCB Design"

Date: 23-08-2019

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?	✓				
2	Is the certification program well planned or not?	✓				
3	Lecture makes objectives clear?		✓			
4	Lecture speaks clearly and audibly?		✓			
5	Lecture explains with exaples clearly?		✓			
6	Is you are doubts clarified or not?	✓				

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: *V. Gayatri*
Roll No : *188B1A0439*
Topic : Certificate Program on "PCB Design"

Date: 23-08-2019

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?		✓			
2	Is the certification program well planned or not?	✓				
3	Lecture makes objectives clear?	✓				
4	Lecture speaks clearly and audibly?		✓			
5	Lecture explains with exaples clearly?		✓			
6	Is you are doubts clarified or not?		✓			

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

N. S.
Student Signature

N. S.
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M. H

Student Signature



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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: *M. Harish*
Roll No : *188BIA0452*
Topic : Certificate Program on "PCB Design"

Date: 23-08-2019

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?	✓				
2	Is the certification program well planned or not?		✓			
3	Lecture makes objectives clear?	✓				
4	Lecture speaks clearly and audibly?	✓				
5	Lecture explains with examples clearly?	✓				
6	Is your doubts clarified or not?	✓				

5-Excellent

4-Good

3-Average

2-Poor

1- No comment

M. H

Student Signature

Veerabhadra
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Department of Electronics and Communication Engineering


Certificate program Feedback Analysis

Topic : Certification program on " PCB Design"
Resource Person : **F.Daniel**
Director, center for Electronics System Design, Vijayawada
Dates : 19-08-2019 to 23-08-2019
Venue : Seminar Hall
Targeted Students : II Year students

S.No	No. of students Participated	No. of students given feedback	Feedback %
1	129	129	100%


Coordinator


Head of the Department


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HEAD OF THE DEPARTMENT
Department of ECE
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P.-523 272



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Department of Electronics and Communication Engineering

Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM

Name of the Student: _____

ROLL Number: _____

1. Which phenomenon is not reduced by the circuit paths of lowest impedances especially provided by power and return planes for shielding purposes?

- a) Radiation
- b) Convection
- c) Noise
- d) Crosstalk

[]

2. High current circuits are purposely located or placed near the edge of PCB in accordance to the supply lines for _____

- a) Removal of heat
- b) Isolation of stray current
- c) Reduction of path length
- d) All of the above

[]

3. Which among the below stated soldering methods is also renowned as 'High Frequency Resistance Soldering'?

- a) Iron Soldering
- b) Furnace Soldering
- c) Torch Soldering
- d) Electrical Soldering

[]

4. Which among the below mentioned approaches belongs to the category of In-circuit Testing?

- a) Impedance Testing
- b) Component Testing
- c) Apply Signal and check output
- d) All of the above

[]

5. Which type of solderability testing is carried out for the generation of solder sample due to immersion of wire or sheet metal specimen in a bath of molten solder?

- a) Solder Bath Testing
- b) Meniscus Rise Testing
- c) Solder Iron Testing
- d) None of the above

[]

6. What is/are the necessity/ies to provide guarding to precision differential amplifiers?

- a) To increase leakage resistance
- b) To reduce capacitance between signal conductors & ground
- c) Both a and b
- d) None of the above

[]

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Department of Electronics and Communication Engineering

7. Which among the below mentioned assertions is not a way of cross-talk reduction while designing digital PCBs?

- a) Decrease in the distance between conductors
- b) Shielding of clock lines with guard strips
- c) Reduction in the loop area of circuits
- d) Avoid running of parallel traces for longer distances especially for asynchronous signals[]

8. Which among the below mentioned packages does not belong to the category of 'Small Outline Package'?

- a) SO
- b) SOP
- c) SOT
- d) SON []

9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?

- a) Analog side to analog ground
- b) Digital side to digital ground
- c) Use of separate power supply and connection of their ground leads to single point reference
- d) Reduction of inductive loop area between power and return traces []

10. Which among the below stated devices/equipments are preferred for elimination of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?

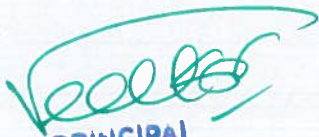
- a) Coupling capacitor
- b) Decoupling capacitor
- c) Snubber circuits
- d) All of the above []

11. Which among the below specified condition is precise in the crosstalk verification mechanism using logic flow in opposite direction with the limit of avoiding dangerous interference in digital PCB designing? []

- a) $Z_{\text{even}} > Z_{\text{odd}}$
- b) $Z_{\text{odd}} \geq 0.5 Z_{\text{even}}$
- c) $Z_{\text{odd}} \geq 0.8 Z_{\text{even}}$
- d) $Z_{\text{odd}} = Z_{\text{even}}$

12. Which terminology of PCB represents a thin photo-sensitive polymer by supporting photographic pattern of single traces or IC pads for etching?

- a) Prepreg
- b) Etching
- c) Photo-resist
- d) Solder mask []


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13. Which problems are about to occur if PCB is not designed properly in a confined manner for digital circuits?

- A. Diffraction
- B. Refraction
- C. Ground & Supply-line Noise
- D. Electromagnetic Interference

[]

- a) A & B
- b) B & C
- c) C & D
- d) A, B, C, D

14. Which among the following assists in obtaining the desired value of wave impedance in reflection phase while designing digital PCBs?

- A. Width of signal lines
- B. Distance between signal line and ground line
- C. Signal Delays
- D. Double Pulsing

- a) A & B
- b) B & C
- c) C & D
- d) A, B, C, D

[]

15. What should be the resistance of 0.6 mm wide conductor with 15 cm length and 25 μm thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$ (at 20° C))

- a) 118.2 m Ω
- b) 138.2 m Ω
- c) 172.4 m Ω
- d) 192.4 m Ω

[]

16. The actual cost of PCB can be evaluated on the basis of _____

- a) PCB size & material
- b) Number of layers
- c) Vias on PCB
- d) All of the above

[]

17. Which factors contribute to the occurrence of mechanical stress?

- a) Resonance
- b) Cracked Solder Joints
- c) Both a and b
- d) None of the above

[]

18. Which type of PCB requires minimum soldering on component side in order to avoid replacement oriented difficulties?

- a) Single-sided PCB
- b) Double-sided PCB
- c) Both a and b
- d) None of the above

[]

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19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?

- a) Increase in self-inductance
- b) Reduction in self-inductance
- c) Stability in self-inductance
- d) None of the above

[]

20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

- a) The use of a 3D component
- b) The use of a 3D component and component clearance rule
- c) The use of a courtyard
- d) The use of a courtyard and a component clearance rule

[]

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ANSWERS

1. Answer: Convection
2. Answer: Removal of heat
3. Answer: Electrical Soldering
4. Answer: All of the above
5. Answer: Meniscus Rise Testing
6. Answer: Both a and b
7. Answer: Decrease in the distance between conductors
8. Answer: SON
9. Answer: Reduction of inductive loop area between power and return traces
10. Answer: Decoupling capacitor
11. Answer: $Z_{\text{odd}} \geq 0.8 Z_{\text{even}}$
12. Answer: Photo-resist
13. Answer: C & D
14. Answer: A & B
15. Answer: $172.4 M\omega$
16. Answer: All of the above
17. Answer: Both a and b
18. Answer: Double-sided PCB
19. Answer: Reduction in self-inductance
20. Answer: The use of a courtyard and a component clearance rule

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Department of Electronics and Communication Engineering

Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM

Name of the Student: Kari Sahithi

ROLL Number:
188B1A0475

18
20

1. Which phenomenon is not reduced by the circuit paths of lowest impedances especially provided by power and return planes for shielding purposes?

- a) Radiation
- b) Convection
- c) Noise
- d) Crosstalk

[b] ✓

2. High current circuits are purposely located or placed near the edge of PCB in accordance to the supply lines for _____

- a) Removal of heat
- b) Isolation of stray current
- c) Reduction of path length
- d) All of the above

[a] ✓

3. Which among the below stated soldering methods is also renowned as 'High Frequency Resistance Soldering'?

- a) Iron Soldering
- b) Furnace Soldering
- c) Torch Soldering
- d) Electrical Soldering

[d]

4. Which among the below mentioned approaches belongs to the category of In-circuit Testing?

- a) Impedance Testing
- b) Component Testing
- c) Apply Signal and check output
- d) All of the above

[d] ✓

5. Which type of solderability testing is carried out for the generation of solder sample due to immersion of wire or sheet metal specimen in a bath of molten solder?

- a) Solder Bath Testing
- b) Meniscus Rise Testing
- c) Solder Iron Testing
- d) None of the above

[b] ✓

6. What is/are the necessity/ies to provide guarding to precision differential amplifiers?

- a) To increase leakage resistance
- b) To reduce capacitance between signal conductors & ground
- c) Both a and b
- d) None of the above

[c] ✓

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7. Which among the below mentioned assertions is not a way of cross-talk reduction while designing digital PCBs?

- a) Decrease in the distance between conductors
- b) Shielding of clock lines with guard strips
- c) Reduction in the loop area of circuits
- d) Avoid running of parallel traces for longer distances especially for asynchronous signals [A] ✓

8. Which among the below mentioned packages does not belong to the category of 'Small Outline Package'?

- a) SO
- b) SOP
- c) SOT
- d) SON [d] ✓

9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?

- a) Analog side to analog ground
- b) Digital side to digital ground
- c) Use of separate power supply and connection of their ground leads to single point reference
- d) Reduction of inductive loop area between power and return traces [d] ✓

10. Which among the below stated devices/equipments are preferred for elimination of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?

- a) Coupling capacitor
- b) Decoupling capacitor
- c) Snubber circuits
- d) All of the above [c] ✗

11. Which among the below specified condition is precise in the crosstalk verification mechanism using logic flow in opposite direction with the limit of avoiding dangerous interference in digital PCB designing? [a] ✗

- a) $Z_{\text{even}} > Z_{\text{odd}}$
- b) $Z_{\text{odd}} \geq 0.5 Z_{\text{even}}$
- c) $Z_{\text{odd}} \geq 0.8 Z_{\text{even}}$
- d) $Z_{\text{odd}} = Z_{\text{even}}$

12. Which terminology of PCB represents a thin photo-sensitive polymer by supporting photographic pattern of single traces or IC pads for etching?

- a) Prepreg
- b) Etching
- c) Photo-resist [c] ✓
- d) Solder mask


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13. Which problems are about to occur if PCB is not designed properly in a confined manner for digital circuits?

- A. Diffraction
- B. Refraction
- C. Ground & Supply-line Noise
- D. Electromagnetic Interference

[C] ✓

- a) A & B
- b) B & C
- c) C & D
- d) A, B, C, D

14. Which among the following assists in obtaining the desired value of wave impedance in reflection phase while designing digital PCBs?

- A. Width of signal lines
- B. Distance between signal line and ground line
- C. Signal Delays
- D. Double Pulsing

[A] ✓

- a) A & B
- b) B & C
- c) C & D
- d) A, B, C, D

15. What should be the resistance of 0.6 mm wide conductor with 15 cm length and 25 μm thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$ (at 20° C)

- a) 118.2 m Ω
- b) 138.2 m Ω
- c) 172.4 m Ω
- d) 192.4 m Ω

[C] ✓

16. The actual cost of PCB can be evaluated on the basis of _____

- a) PCB size & material
- b) Number of layers
- c) Vias on PCB
- d) All of the above

[d] ✓

17. Which factors contribute to the occurrence of mechanical stress?

- a) Resonance
- b) Cracked Solder Joints
- c) Both a and b
- d) None of the above

[c] ✓

18. Which type of PCB requires minimum soldering on component side in order to avoid replacement oriented difficulties?

- a) Single-sided PCB
- b) Double-sided PCB
- c) Both a and b
- d) None of the above

[b] ✓



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19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?

- a) Increase in self-inductance
- b) Reduction in self-inductance
- c) Stability in self-inductance
- d) None of the above

[b] ✓

20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

- a) The use of a 3D component
- b) The use of a 3D component and component clearance rule
- c) The use of a courtyard
- d) The use of a courtyard and a component clearance rule

[d] ✓

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Department of Electronics and Communication Engineering

19
20

Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM

Name of the Student: K. madhavi

ROLL Number: 188BA0420

1. Which phenomenon is not reduced by the circuit paths of lowest impedances especially provided by power and return planes for shielding purposes?

- a) Radiation
- b) Convection
- c) Noise
- d) Crosstalk

[b] ✓

2. High current circuits are purposely located or placed near the edge of PCB in accordance to the supply lines for _____

- a) Removal of heat
- b) Isolation of stray current
- c) Reduction of path length
- d) All of the above

[a] ✓

3. Which among the below stated soldering methods is also renowned as 'High Frequency Resistance Soldering'?

- a) Iron Soldering
- b) Furnace Soldering
- c) Torch Soldering
- d) Electrical Soldering

[d] ✓

4. Which among the below mentioned approaches belongs to the category of In-circuit Testing?

- a) Impedance Testing
- b) Component Testing
- c) Apply Signal and check output
- d) All of the above

[c] ✗

5. Which type of solderability testing is carried out for the generation of solder sample due to immersion of wire or sheet metal specimen in a bath of molten solder?

- a) Solder Bath Testing
- b) Meniscus Rise Testing
- c) Solder Iron Testing
- d) None of the above

[b] ✓

6. What is/are the necessity/ies to provide guarding to precision differential amplifiers?

- a) To increase leakage resistance
- b) To reduce capacitance between signal conductors & ground
- c) Both a and b
- d) None of the above

[c] ✓

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7. Which among the below mentioned assertions is not a way of cross-talk reduction while designing digital PCBs?

- a) Decrease in the distance between conductors
- b) Shielding of clock lines with guard strips
- c) Reduction in the loop area of circuits
- d) Avoid running of parallel traces for longer distances especially for asynchronous signals [a] ✓

8. Which among the below mentioned packages does not belong to the category of 'Small Outline Package'?

- a) SO
- b) SOP
- c) SOT
- d) SON [d] ✓

9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?

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- b) Digital side to digital ground
- c) Use of separate power supply and connection of their ground leads to single point reference
- d) Reduction of inductive loop area between power and return traces [d] ✓

10. Which among the below stated devices/equipments are preferred for elimination of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?

- a) Coupling capacitor
- b) Decoupling capacitor
- c) Snubber circuits
- d) All of the above [b] ✓

11. Which among the below specified condition is precise in the crosstalk verification mechanism using logic flow in opposite direction with the limit of avoiding dangerous interference in digital PCB designing? [c] ✓

- a) $Z_{\text{even}} > Z_{\text{odd}}$
- b) $Z_{\text{odd}} \geq 0.5 Z_{\text{even}}$
- c) $Z_{\text{odd}} \geq 0.8 Z_{\text{even}}$
- d) $Z_{\text{odd}} = Z_{\text{even}}$

12. Which terminology of PCB represents a thin photo-sensitive polymer by supporting photographic pattern of single traces or IC pads for etching?

- a) Prepreg
- b) Etching
- c) Photo-resist
- d) Solder mask [c] ✓

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Department of Electronics and Communication Engineering

13. Which problems are about to occur if PCB is not designed properly in a confined manner for digital circuits?

- A. Diffraction
- B. Refraction
- C. Ground & Supply-line Noise
- D. Electromagnetic Interference

- a) A & B
- b) B & C
- c) C & D
- d) A, B, C, D

[c] ✓

14. Which among the following assists in obtaining the desired value of wave impedance in reflection phase while designing digital PCBs?

- A. Width of signal lines
- B. Distance between signal line and ground line
- C. Signal Delays
- D. Double Pulsing

- a) A & B
- b) B & C
- c) C & D
- d) A, B, C, D

[a] ✓

15. What should be the resistance of 0.6 mm wide conductor with 15 cm length and 25 μm thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$ (at 20° C))

- a) 118.2 m Ω
- b) 138.2 m Ω
- c) 172.4 m Ω
- d) 192.4 m Ω

[c] ✓

16. The actual cost of PCB can be evaluated on the basis of _____

- a) PCB size & material
- b) Number of layers
- c) Vias on PCB
- d) All of the above

[d] ✓

17. Which factors contribute to the occurrence of mechanical stress?

- a) Resonance
- b) Cracked Solder Joints
- c) Both a and b
- d) None of the above

[c] ✓

18. Which type of PCB requires minimum soldering on component side in order to avoid replacement oriented difficulties?

- a) Single-sided PCB
- b) Double-sided PCB
- c) Both a and b
- d) None of the above

[b] ✓


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19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?

- a) Increase in self-inductance
- b) Reduction in self-inductance
- c) Stability in self-inductance
- d) None of the above

[b] ✓

20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

- a) The use of a 3D component
- b) The use of a 3D component and component clearance rule
- c) The use of a courtyard
- d) The use of a courtyard and a component clearance rule

[d] ✓

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Certificate Program on PCB Design Assessment Marks

A.Y : 2019-2020

Year : II

S. No	Reg. No	Name of the Candidate	Marks
1	168B1A0452	SRIKANTH	19
2	188B1A0401	ABOTHU DIVYA	17
3	188B1A0402	ADIPUDI NAGA LAKSHMI NIKHITHA	18
4	188B1A0403	ATHYALA JOYSIRIYA	17
5	188B1A0404	AVVARU ANUSHA	18
6	188B1A0405	BATTULA RAJANI	19
7	188B1A0406	BELLAMKONDA SRI VENKATESWARA	18
8	188B1A0407	CHIMAKURTHI NAGA LAKSHMI PRAVALLIKA	18
9	188B1A0408	CHALLA SAI LAKSHMI SANTHOSHI	18
10	188B1A0410	DACHARLA SUPRAJA	19
11	188B1A0411	DESIREDDY SUMATHI	18
12	188B1A0412	DIVI SIVANI	19
13	188B1A0413	GANGIREDDY DHANA LAKSHMI	19
14	188B1A0414	GOLLA JYOSHNA	20
15	188B1A0415	JALLI BRIGHTY MANVITHA	16
16	188B1A0416	JASHTI LAKSHMI DEVI	19
17	188B1A0417	KAMJULA NAGA ANUHYA	18
18	188B1A0418	KANAMARLAPUDI DIVYA JYOTHI	19
19	188B1A0419	KAMJULA SUJATHA	17
20	188B1A0420	KONKIMUDUSU MADHAVI	19
21	188B1A0421	KOPPOLU SATHVIKA	16
22	188B1A0422	KOTHURI KOTI SAI SUPRIYA	18
23	188B1A0423	KOTTURU USHA RANI	18
24	188B1A0424	KOYI SRI POOJITHA	18
25	188B1A0425	MAKKENA YASODAMMA	15
26	188B1A0426	MITTA ANJALI	19
27	188B1A0427	MOPIDEVI ANUSHA	18
28	188B1A0428	NALAMALAPU KAVYA	19
29	188B1A0429	PATAN SHAMA	17
30	188B1A0430	PATRI NAGA BHAVANA	19
31	188B1A0431	PERAM SWAPNA	16
32	188B1A0432	PINNINTI NAVYA	16
33	188B1A0433	PITTU SAI BHARGAVI	16
34	188B1A0434	PULAKANAM AKHILA	17


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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
35	188B1A0435	SHAIK SHALIMA	18
36	188B1A0436	SHEIK SALMA	16
37	188B1A0437	THATIKONDA LAVANYA	19
38	188B1A0438	UDALA VENKATA LAKSHMI PRIYA	18
39	188B1A0439	VANKADARI GAYATRI	19
40	188B1A0440	YAKKALA VENKATA NIKHILA	18
41	188B1A0441	YELCHURI LAKSHMI PRASANNA	17
42	188B1A0442	ATTALURI PAVAN RENUKA CHARI	18
43	188B1A0443	BEZAWADA SREEKANTH	17
44	188B1A0444	BOLLA GANGADHAR	18
45	188B1A0445	ELCHURI VINAY KUMAR	19
46	188B1A0446	JAGANNADHAM NAVEEN KUMAR	18
47	188B1A0447	KANAMARLAPUDI SATYAVARDHAN	18
48	188B1A0448	KARNA PAVAN KUMAR REDDY	17
49	188B1A0449	KURAPATI VIDYASAGAR	19
50	188B1A0450	MALLAVARAPU VENKATA RAMI REDDY	20
51	188B1A0451	MALASANI VENKATA VAMSI KRISHNA	20
52	188B1A0452	MEDA HARISH	16
53	188B1A0453	P U V N S M JANAKIRAM SHARMA	19
54	188B1A0454	RALLAPALLE VEERA VISHNU	16
55	188B1A0455	SHAIK ABDHUL AZEESH	20
56	188B1A0456	SHAIK ANIL KUMAR	16
57	188B1A0457	THOTA GNAN VAMSI SAI KRISHNA	19
58	188B1A0458	THOTA GOPI	18
59	188B1A0459	VAKA PRAVEEN KUMAR REDDY	19
60	188B1A0461	ALLU LAKSHMI	18
61	188B1A0462	BOLLISSETTY JYOTHIRMAY	17
62	188B1A0463	CHAKKA ANUHYA	17
63	188B1A0464	CHAKRALA MANIMALA	17
64	188B1A0465	CHEEDELLA DIVYASRI	19
65	188B1A0466	CHOUTA VYSHNAVI	16
66	188B1A0467	DASARI AMRUTHA	18
67	188B1A0468	DUMPA ANJALI	18
68	188B1A0469	ENIKAPATI ANITHA	19
69	188B1A0470	ENIKAPATI ANUSHA	18
70	188B1A0471	GAJJALA SANDHYA	19
71	188B1A0472	GARLAPATI KAMALA KUMARI	20


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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
72	188B1A0473	GOLI SOWMYA	18
73	188B1A0474	KAMJULA VASANTHA LAKSHMI	17
74	188B1A0475	KARI SAHITHI	18
75	188B1A0476	KOPPARTHI HYMAVATHI	19
76	188B1A0477	KOTA RENUKA	18
77	188B1A0478	LEBAKA SASI BALA	18
78	188B1A0479	MEDIDA MOUNIKA	17
79	188B1A0480	MOPIDEVI NAGA NANDINI	18
80	188B1A0481	MULI BINDU	16
81	188B1A0482	NARIPEDDI MEGHANA	16
82	188B1A0484	PATHAN SHYLABANU	17
83	188B1A0485	PERLA PRAVALLIKA	19
84	188B1A0486	PINISSETTY RAJITHA	20
85	188B1A0487	SANDIREDDY SOUNDARYA	16
86	188B1A0488	SHAIK SHARMILA	19
87	188B1A0489	SOMINENI JYOTHSNA	16
88	188B1A0490	TANGA SAI RAMYA	20
89	188B1A0491	TURIMELLA SRAVANI	20
90	188B1A0492	VEMURI SHAHINA	16
91	188B1A0493	YALLATURI DEVI SIRISHA	19
92	188B1A0494	ANCHULA VENKATESWARLU	18
93	188B1A0495	B BHARATH KUMAR REDDY	19
94	188B1A0496	BETHAMSETTY VAMSIKRISHNA SAISRINIVAS	17
95	188B1A0497	BODDU JANARDHAN RAO	19
96	188B1A0498	BUKKA PRABHU TEJA	16
97	188B1A0499	BURLA PRANEETH REDDY	18
98	188B1A04A0	DAMERLA VAMSI KRISHNA	18
99	188B1A04A1	DHARMAVARAPU THARUN KUMAR	18
100	188B1A04A2	GADDE RAJESH	15
101	188B1A04A3	KARAMSETTY J CH P VENKATA SAI MANEESH	19
102	188B1A04A4	KOCHARLA KARTHIK	18
103	188B1A04A5	KOLLIPARA PAVAN KALYAN	19
104	188B1A04A6	MANDLA SRINIVASULU	17
105	188B1A04A7	NALLAGUNDLA VINAY KUMAR	19
106	188B1A04A8	PASUPULETI GOPI KRISHNA	19
107	188B1A04B0	SEELAM RAMU	19
108	188B1A04B1	SHAIK HEMANTH BABU	20


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Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
109	188B1A04B2	TANGUTURI KUMAR	17
110	188B1A04B3	VADITHE SIVA PRASAD NAIK	18
111	188B1A04B4	VAIDALA GIREESH REDDY	16
112	188B1A04B5	VELICHERLA PRABHAKAR REDDY	16
113	188B1A04B6	VUTUKURI BALASURYA PRADEEP	17
114	188B1A04B7	YADALA BENNI	19
115	188B1A04B8	KESANA AISHWARYA BHAVANI	20
116	188B1A04B9	BATTINI VENKATA PRASAD	19
117	198B5A0401	APPALA SARVANI	18
118	198B5A0402	BANDLA VENKATA NIKHITHA	18
119	198B5A0403	PULICHARLA DEEPIKA	19
120	198B5A0404	VEGURI SWATHI	19
121	198B5A0405	ANKIREDDY VAMSI	18
122	198B5A0406	ARLA CHANDRA SHEKHAR	19
123	198B5A0407	GORREMUCHHU SANDEEP	17
124	198B5A0408	GUNIMINI SAI	19
125	198B5A0409	KALLURI SARATH	20
126	198B5A0410	PULUGU DEVENDAR REDDY	20
127	198B5A0411	PUNNEPALLI RAKESH	16
128	198B5A0412	SHAIK AZIS	19
129	198B5A0413	NARAYANAM SREE VASU	19

S. V. Srinivas
Coordinator

S. V. Srinivas
PRINCIPAL
RISE KRISHNA SAI GANDHI
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S. V. Srinivas
HOD
HEAD OF THE DEPARTMENT
Department of E.C.E
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P.-523 272

**RISE KRISHNA SAI GANDHI GROUP
OF INSTITUTIONS: ONGOLE
DEPARTMENT OF ECE**

**[Certificate program on PCB Design
19-08-2019 to 23-08-2019]**

The Certificate Program conducted by ECE department on 19th - 23th August 2019 in
RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS in association with
Center for Electronics System Design (CESD)

Department of Electronics & Communication Engineering


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Objectives of conducting Certificate program

- To make students learn and interact with renowned industry experts.
- Make Students to receive an unparalleled education on the art of **PCB Designing Certificate program** with personal one on one attention.
- To make every student an expert in designing their own **PCB board** which would be very useful for developing their own projects.

Overview about Certificate Program:

The aim of this **Certificate Program** is to make the students learn the designing and manufacturing of a printed circuit board using open source KICAD PCB design software and with various active and passive components such as Regulators, Diodes, Resistors, Capacitors, Inductors, Switches, e.t.c.

Technical Support:

The **Certificate Program** was conducted in collaboration with Center for Electronics System Design (CESD) from Vijayawada. The company has a fast growth in PCB designing. The company's director Mr. Finney Daniel accompanied with Seven Trainers attended the Certificate Program for guiding the students in learning the technologies of the PCB Design Certificate Program. They have taken about 32 hours of theoretical and practical sessions.

Department of ECE:


Department of ECE has taken the opportunity to conduct the in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS. As the theme of the Certificate Program is the core for the department, it's a nice opportunity for the students to learn the technology and to implement that practically.

Technical Report on Certificate Program:

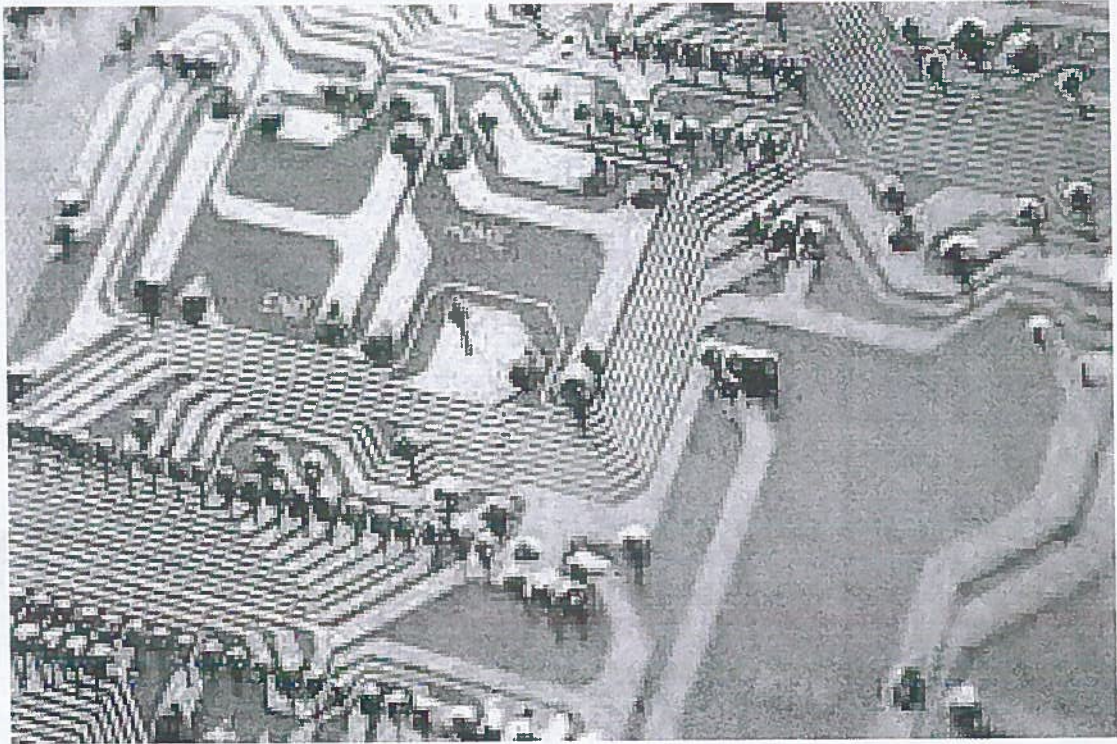
The Technical team of Center for Electronics System Design (CESD) has described the entire designing process in a step by step procedure.

1. Basic PCB Concepts

First of all they have given the concepts which will be very helpful for designing the PCB practically, using some power point presentations. In this theoretical explanation part they have explained about the KI-CAD software and the use of software for further practical implementation in designing the PCB. They have also

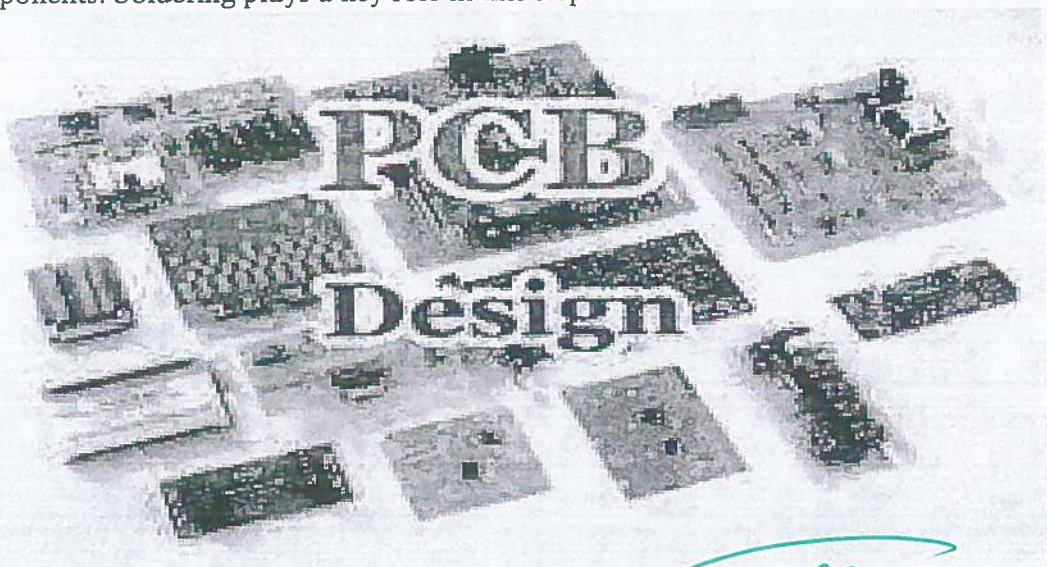

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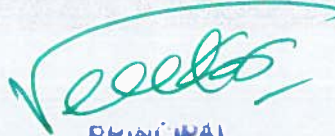
given a briefing about active and passive electronic components which they will be using in a PCB.



2. Editing and Routing

Editing and Routing is the basic step and it is one of the important step for designing a PCB. Editing and Routing gives the circuit layout from one component to the other components. Soldering plays a key role in this step.




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3. Creation of Library and Components & Report Generation

This is a step done using KI-CAD tools. In this step the components in the circuit and the respective libraries are selected in this software. So that the required circuit will be designed in the software and a print of the same will be taken on a sheet. The same print will be useful for the further process.

4. Toner Transfer Method

This is the step where the designed circuit will be pasted on the wafer and this will be passed through a temperature of about 160 to 180 degrees so that the tracks of the circuit will be remained on the wafer. The tracks will be a conductive type.

5. Drilling Technique

The board will be drilled with holes where the components have to be placed; the holes will be drilled in the board depending on the terminals available for the components in the design. The hole should be in the size so that the terminal has to be freely placed in the hole.

6. Soldering Technique

The components that are placed in the board should be soldered to the track so that the circuit is connected as per the design. After this step the engraved PCB will be ready to use.

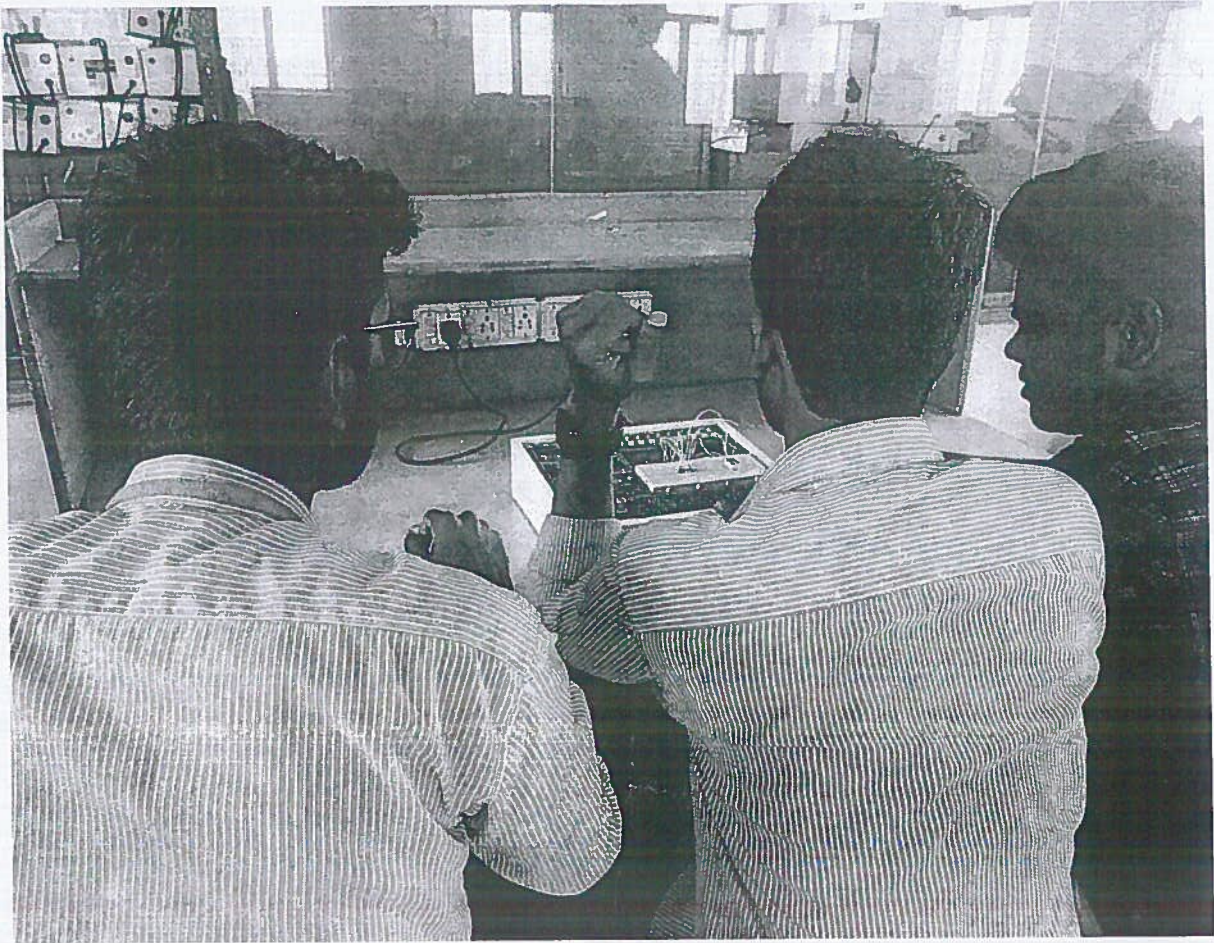
The Department conducted test on PCB Design for Electronic components and all project models are exhibited in the respected department

Student Response

Almost 129 students had taken part in the Certificate Program. All the students responded that they have learned and had hands on experience in designing a PCB. They are very excited in participation in this Certificate Program and requested for more Certificate Program in similar way so that they can simultaneously gain the practical knowledge.



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Distribution of Certificates

At the last day question answer session and certificate distribution function started on 4:30 PM. Feedbacks regarding workshop are provided by various students.

All the students were awarded with a participation certificate from the company Center for Electronics System Design(CESD). Principal Dr.K.V.Subrahmanyam garu awarded the certificates to all the students by hand. He personally congratulated every student for participating in the event and making it successful.

Vote of Thanks

Mr.S V Ravi Kumar beloved HOD of ECE Department thanked every student for their active participation and interest in participating in the Certificate Program and mentioned about the activities conducted in the college by the department. He promised



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that department will continue its assistance in conducting these sorts of Certificate Programs and seminars in future.

He thanked the technical support given by **Center for Electronics System Design (CFSD)**. He personally felt very happy for the response of the company and satisfied with the way they conducted the Certificate Program.

He mentioned about the marvelous support given by the Principal Dr.K.V.Subrahmanyam garu to the department in conducting these Certificate Program. He also thanked for the personal interest taken by him in encouraging the department in all aspects.

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NH-16, Valluru, Ongole, Prakasam (District)-523272
Department of Electronics and Communication Engineering

Date: 23-08-2019.

CLOSING REPORT

To,
The Principal,
RISE Krishna Sai Gandhi Group of Institutions.

As per the approved schedule, the ECE department has conducted a Certificate Program on "PCB Design" at ECE Seminar hall from 19-08-2019 to 23-08-2019. 129 students of II ECE have participated in this program. Sri F.Daniel, Director, Center for Electronics Systems Design (CESD), Vijayawada, AP, acted as the resource person for this program.

Main issues addressed:

1. Basic PCB Concepts
2. Editing and Routing
3. Creation of Library and Components & Report Generation
4. Toner Transfer Method
5. Drilling Technique
6. Soldering Technique

We are expecting your support in future also. Thanking you sir,

Yours faithfully,

Sare
Coordinator

Reddy
PRINCIPAL
RISE KRISHNA SAI GANDHI
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S.V. Daniel
HOD
HEAD OF THE DEPARTMENT
Department of E.C.E.
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of Institutions, VALLURU, A.P. 523 272