RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE

Department of Electronics and Communication Engineering

Certificate Program

On

"PCB Design "

Date: 24th to 28th September 2018

Finney Daniel

Dirctor,center for electronics system design
Vijayawada

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GROUP OF INSTITUTIONS
VALLURU:: ONGOLE.

RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

(Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada)
NH-16, Valluru, Ongole, Prakasam (District)-523272

Valluru,

Date: 11-09-2018

To

F.Daniel,
Dirctor,Center for Electronics System Design,
Vijayawada.

Dear Sir,

Subject: Inviting for Certificate program - Reg.

Greetings from RISE Krishna Sai Gandhi Group of Institutions, Ongole

As per the discussion with Dr.K.V.Subrahmanyam , Principal, of our Institute, I hereby take this opportunity to invite you to conduct the Certificate program on **PCB Design** " From 24-09-2018 to 28-09-2018.

You are requested to interact and provide guidance to our II B.Tech students, who are looking forward to their bright career ahead. I will feel honored by your gracious presence at our organization. I believe that your lecture will help our students and faculty members to explore knowledge.

Thanking you in anticipation.

Yours sincerely,

Principal

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Finney Daniel

Managing Director

Center for Electronics System Design

Personal Summary

Finney Daniel has a record of organizing Institutional Industry oriented up-gradation programs for undergraduates. Experienced in delivering recent trend technologies to the personnel in vivid methodologies. Providing a lawn of possibilities in the specified area which strengthen the personnel in growing the skills required for their success in the present day competence. He has experience as a guest lecturer, assistant professor and a research fellow. His main interest in this has been to prove the potential and ability of the personnel.

Professional Summary

- Delivered services as Guest Lecturer for VLSI in Andhra University College of Engineering.
- Worked as Assistant Professor in couple of Engineering Colleges.
- As Junior Research Fellow in Defence Research & Development Laboratory.

Areas of Expertise

- **Product Development:** Evolving modules that enable a final product meeting the End- User requirements and facilitate easy utility of the product
- **Project Management:** Maintaining strategic planning and supporting the team in delivering Robust Models by providing employ friendly platform.
- **Organizing Training Sessions:** Planned tabulation for training and hands on expertise for the personnel under training.

Professional Skills and Competencies

- Strong knowledge on Software tools like QUARTUS, Xilinx, Cadence, Tanner- EDA, Mentor-Graphics required for VLSI.
- Good knowledge on hardware design and development includes familiarity in Embedded System tools and PCB design tools like MPLAB Xpress IDE, KEIL, Micro-c, ZUKEN- Cadstar, Eagle, Express-PCB.

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Key Roles

- Academic Director for KR's Educational Society.
- Coordinator for Technical Symposium in Holy Mary Group of Institutions.
- Organized Workshops on Verilog, PCB Design, Prototyping, Embedded Systems, Product Design and Development.

Qualification

- Master of Technology in VLSI-System Design from JNTU-Kakinda.
- PG Diploma in Electronic Product Design from Electronics System Design and Manufacturing (ESDM, Govt. of India).
- Graduation in Electronics & Communication Engineering from CJITS, JNTU- Hyderabad.
- Graduation in Bachelor of Science in Mathematics from Andhra University.

Personal Details

- Born on 21st June 1987 in Visakhapatnam.
- Indian citizen and can speak Hindi, English, Telugu.

References - Available on Request.

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NH-16, Valluru, Ongole, Prakasam (District)-523272
Department of Electronics and Communication Engineering

PROPOSAL FORM

SUB: Certificate program -Program.

TO THE SECRETARY/CORRESPONDENT THROUGH PRINCIPAL FOR KIND APPROVAL

1	NAME OF THE INSTITUTION	**Rise Krishna Sai Gandhi Group of Institutions**
2	NAME OF THE DEPARTMENT	Electronics & Communication Engineering
3	TITLE OF THE PROGRAMME	Certificate program
4	NAME OF THE PROGRAMME	Certificate program on **" PCB Design for Electronic Designs"**
5	OBJECTIVE OF THE PROGRAMME	To bring the exposure in the PCB Design.
6	DETAILS OF RESOURCE PERSON(S)& CV ATTACHED.	Finney Daniel Director, center for electronics system design Vijayawada.
7	PROPOSED DATE(S)/ACADEMIC YEAR	24-09-2018 to 28-09-2018
8	DURATION OF THE PROGRAMME	FIVE DAY
9	VENUE	Seminar Hall
10	TARGETS	II ECE students
11	No. OF PARTICIPANTS	118 Students
12	REGISTRATION FEE	Free
13	NAME OF PROGRAMME CO ORDINATOR(S)	Mr. K.Nagahanuma Chari
14	NAME OF THE STUDENTS COORDINATOR(S)	1.Ms. G.Manisha (178B1A0411) 2.Mr.Pakala Nikhil Gopal (178B1A04B1)

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15	SOURCE OF FUND IDENTIFIED	Management
16	MANAGEMENT CONTRIBUTION REQUIRED	YES
17	PROPOSAL PREPARED BY	Mr.K.Nagahanuma Chari (CO-ORDINATOR)

Coordinator

HOD

HEAD OF THE DEPARTMENT
Department of E.C.E.
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P.-523 272

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NH-16, Valluru, Ongole, Prakasam (District)-523272
Department of Electronics and Communication Engineering

Valluru,
Date: 21-09-2018.

CIRCULAR

This is to inform II B.Tech students and faculty that there will be a 5-Day Certificate program on **"PCB Design"** from **24-09-2018 to 28-09-2018** by **F.Daniel**, Dirctor,Center for Electronics System Design, Vijayawada.

HOD

Copy to:

Principal

Staff Circular

Students of ECE II year

ECE Department Notice Boards

HEAD OF THE DEPARTMENT
Department of E.C.E
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of Institutions,VALLURU,A.P.-523 272

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Department of Electronics and Communication Engineering

Certificate Program on "PCB Design"

Date: 24th to 28th Sep 2018

SCHEDULE FROM 24-09-2018 TO 28-09-2018

S. No	Program List	Timing	
		From	To
DAY – 01 (24-09-2018)			
1	Program started	09.00 AM	--
2	Lamp lighting	09.00 AM	09.10 AM
3	Principal speech	09.10 AM	09.25 AM
4	HOD Introduction about PCB Design	09.25 AM	09.35 AM
5	Tea Break	09.35 AM	10.00 AM
6	Introduction about PCB concepts	10.00 AM	01.00 PM
7	Lunch Break	01.00 PM	01.45 PM
8	KI-CAD Software Practical Section	01.45 PM	05.00 PM
DAY – 02 (25-09-2018)			
9	Concepts of PCB Designing, PCB Materials, Layers	09.00 AM	12.15 PM
10	Lunch Break	12.15 PM	01.00 PM
11	Multilayer Concepts	01.00 PM	05.00 PM
DAY – 03 (26-09-2018)			
12	PADSTACK	09.00 AM	12.15 PM
13	Lunch Break	12.15 PM	01.00 PM
14	Schematic entry KI-CAD tools	01.00 PM	05.00 PM
DAY – 04 (27-09-2018)			
15	Drawing a schematic FLAT	09.00 AM	12.15 PM
16	Lunch Break	12.15 PM	01.00 PM
17	BOM. Net list generation	01.00 PM	05.00 PM
DAY – 05 (28-09-2018)			
18	Designing Boards	09.00 AM	12.15 PM
19	Lunch Break	12.15 PM	01.00 PM
20	Drawing a schematic HIERARCHICAL Design	01.00 PM	04.15 PM
21	Certificate Program Exam	04.15 PM	04.45 PM
22	Vote of Thanks	04.45 PM	05.00 PM

Coordinator

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: CH. Hemanth kumar

Roll No : 178B1A04A0

Date: 28-09-2018

Topic : Certificate Program on "PCB Design"

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?	✓				
2	Is the certification program well planned or not?		✓			
3	Lecture makes objectives clear?		✓			
4	Lecture speaks clearly and audibly?		✓			
5	Lecture explains with exaples clearly?	✓				
6	Is you are doubts clarified or not?	✓				

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

Student Signature

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Student Signature

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: N. Thriveni
Roll No : 178B1A0430
Topic : Certificate Program on "PCB Design"

Date: 28-09-2018

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?	✓				
2	Is the certification program well planned or not?		✓			
3	Lecture makes objectives clear?	✓				
4	Lecture speaks clearly and audibly?		✓			
5	Lecture explains with exaples clearly?	✓				
6	Is you are doubts clarified or not?		✓			

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

N. Thriveni
Student Signature

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: P. Gopi

Roll No : 178B1A0432

Date: 28-09-2018

Topic : Certificate Program on "PCB Design"

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?		✓			
2	Is the certification program well planned or not?	✓				
3	Lecture makes objectives clear?	✓				
4	Lecture speaks clearly and audibly?	✓				
5	Lecture explains with exaples clearly?	✓				
6	Is you are doubts clarified or not?	✓				

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

P. Gopi
Student Signature

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Student Feedback Form

Name of the Student: K. Deepthi

Roll No : 178B1A0416

Date: 28-09-2018

Topic : Certificate Program on "PCB Design"

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not ?	✓				
2	Is the certification program well planned or not?	✓				
3	Lecture makes objectives clear?		✓			
4	Lecture speaks clearly and audibly?		✓			
5	Lecture explains with exaples clearly?	✓				
6	Is you are doubts clarified or not?		✓			

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

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K. Deepthi
Student Signature

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DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

CERTIFICATE PROGRAM FEEDBACK ANALYSIS

A.Y: 2018-2019 Year : II B.Tech ECE Date: 28-09-2018

Name of the Certificate Program: PCB Design

S.No	Roll Number	Name	1	2	3	4	5	6
1	178B1A0401	ANNAPAREDDY BHARATHI	5	4	5	4	5	5
2	178B1A0402	ATCHALA CHANDRAKALA	5	4	5	4	5	4
3	178B1A0403	BADUGU AKSHA TEJA	4	5	4	5	5	5
4	178B1A0404	BALAGANI SURYA KANTHAM	4	4	5	4	4	4
5	178B1A0405	BHUMA VENKATA SUNEETHA	5	5	5	4	4	5
6	178B1A0406	BURRA SAI LAKSHMI	4	4	5	4	5	5
7	178B1A0407	CHEREDDY KALPANA	4	4	5	4	4	5
8	178B1A0408	CHINTHAPATLA PAVITHRA	5	4	4	5	5	4
9	178B1A0409	CHIRITOTI LAVANYA	4	4	5	4	4	5
10	178B1A0410	DAMA VENKATA KEERTHANA	4	5	5	4	5	4
11	178B1A0411	G MANISHA	4	4	4	4	5	5
12	178B1A0412	GUNAPANENI VANDANA	4	5	5	4	5	4
13	178B1A0413	GUNDLAPALLI SAMPURNA	4	4	5	4	5	5
14	178B1A0414	JONNALA GADDA ALEKYA	4	5	5	4	5	5
15	178B1A0415	JONNALAGADDA SRUTHI SRAVYA	4	4	5	5	5	5
16	178B1A0416	KADIRI DEEPTHI	5	5	4	4	5	4

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S.No	Roll Number	Name	1	2	3	4	5	6
17	178B1A0417	KAKARLA YAMINI	4	5	5	4	5	5
18	178B1A0418	KANDEPI VENKATA SAI SRAVANI	4	5	4	5	5	4
19	178B1A0419	KOLAPARTI BHAVYASRI	4	4	5	5	5	5
20	178B1A0420	KOLLI MARLA SWETHA	5	5	5	5	5	5
21	178B1A0421	KOMATINENI MOUNIKA	4	5	4	5	5	5
22	178B1A0422	KONIDENA MANISHA	4	4	5	4	5	4
23	178B1A0423	LAKKU MEENAKSHI	4	4	5	4	4	5
24	178B1A0424	LAKSHMISETTY VYSHNAV KEERTHI	5	4	4	4	4	5
25	178B1A0425	MANNAM SRAVANI	5	5	5	5	5	5
26	178B1A0426	MANNEM YAMINI	5	4	5	4	4	5
27	178B1A0427	NARISINGU VASANTHI	5	4	5	5	5	4
28	178B1A0428	NERELLA VENKATA SUSHMA	5	5	4	4	4	5
29	178B1A0429	NUTHALAPATI SRILATHA	4	4	5	4	5	5
30	178B1A0430	NUTHALAPATI THRIVENI	5	4	5	4	5	4
31	178B1A0431	PABBISETTY SAI LAKSHMI VANDANA	5	4	5	4	5	5
32	178B1A0432	PABBISETTY VENKATA RAMYASRI	5	5	4	4	4	5
33	178B1A0433	PERLA VENKATA SAI DEEPTHI	5	5	4	5	4	5
34	178B1A0434	PURIMITLA NAGA LAKSHMI	5	4	4	4	5	4
35	178B1A0435	RENUMALA MOUNIKA	5	5	4	5	5	5
36	178B1A0436	SHAIK SAMINA	5	4	5	4	4	4

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S.No	Roll Number	Name	1	2	3	4	5	6
37	178B1A0437	SHAIK YASMIN	5	5	5	4	4	5
38	178B1A0438	SURA NARAYANAMMA	5	4	5	4	4	5
39	178B1A0439	THANIKANTI HARIKA	4	5	5	4	4	4
40	178B1A0440	UDARAGUDI SAILAJA	5	4	5	4	5	5
41	178B1A0441	YARICHARLA MOUNIKA	5	4	4	5	5	5
42	178B1A0442	ALLA ASHOKREDDY	5	4	5	5	5	5
43	178B1A0443	ALLIKEPALI SRIKANTH	5	5	5	5	5	4
44	178B1A0444	CHAKKA NITHISH	5	4	4	4	4	5
45	178B1A0445	DANNARAPU PAVAN KALYAN	5	5	5	5	5	5
46	178B1A0446	DODDI STEPHEN RAJ	4	5	4	5	4	5
47	178B1A0447	ELURI VENKATA SANJAY	5	4	4	4	5	5
48	178B1A0448	KOPPOLU RAMA KRISHNA	5	5	5	5	5	5
49	178B1A0449	KOTA BRAHMAREDDY	4	4	5	5	4	4
50	178B1A0450	MUVALA SAI VENKATA NAGA VINAY	5	4	5	4	5	5
51	178B1A0451	PABBISETTY MANOJ	5	4	5	4	5	5
52	178B1A0452	POLIMIREDDY MALAKONDA REDDY	5	4	5	5	5	5
53	178B1A0453	PONIGETI HANUMANTHA REDDY	5	4	5	4	5	5
54	178B1A0454	SANKARAMANCHI NAGAMANOHAR SHARMA	5	4	5	4	5	5
55	178B1A0455	SHAIK YASDHANI	5	4	5	4	5	5
56	178B1A0456	SIGHAKOLLI BALA SUBRAMANYAM	5	4	4	4	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
57	178B1A0457	SUNDARASETTY NIKHIL	5	5	5	4	5	5
58	178B1A0458	THOGURU PRAVEEN KUMAR	5	5	5	5	5	5
59	178B1A0459	THOKALA SAMSON	5	5	5	4	5	5
60	178B1A0460	VEMA SAI REVANTH KUMAR	5	4	4	4	5	5
61	178B1A0461	ADAPALA ANUSHA	4	4	5	5	4	4
62	178B1A0462	ALURI RAYELAMMA	5	4	5	4	5	5
63	178B1A0463	BATCHALI VENKATA SAI SARATH PRATYUSHA	5	4	5	4	5	5
64	178B1A0464	BIJJAM SRI LEENA	5	4	4	4	4	5
65	178B1A0465	BIRUDURAJU NAVYA SUSHMA	5	5	5	5	5	5
66	178B1A0466	CHINTHALA KEERTHANA	4	5	4	5	4	5
67	178B1A0467	DEVULAPALLI MAHALAKSHMAMMA	5	4	4	4	5	5
68	178B1A0468	DODDAKA NAGA DEEPTHI	5	4	4	4	5	5
69	178B1A0469	DONEMPUDI ANUSHA	5	5	5	4	5	5
70	178B1A0470	GUJJULA MAHALAKSHMI	5	4	5	4	4	5
71	178B1A0471	GUNJI ANUSHA	5	4	5	4	5	4
72	178B1A0472	KALLAGUNTA VANI VARSHITHA	4	5	5	5	4	5
73	178B1A0473	KARETI PRAVALLIKA	5	4	5	4	5	5
74	178B1A0474	KATTA HYNDAVI	5	5	5	5	4	5
75	178B1A0475	KELAM RAMA DEVI	5	5	4	5	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
76	178B1A0476	MADALA VENKATA SAI LAKSHMI	5	5	5	4	5	4
77	178B1A0477	MARELLA VENKATA SIREESHA	5	4	5	5	5	4
78	178B1A0478	MOLAKALAPALLI MADHAVI LATHA	5	4	5	4	5	5
79	178B1A0479	MONDRU MARY AMULYA	5	5	5	4	5	5
80	178B1A0480	MOTHUKURI ANILA	5	4	4	4	5	5
81	178B1A0481	MULAGANI UMA DEVI	5	4	5	5	5	4
82	178B1A0482	NELAMALLI SUREKHA	4	5	5	4	5	5
83	178B1A0483	NUKATHOTI DEENAMMA	5	5	5	4	5	5
84	178B1A0484	PATHAKAMURI VIJAYA NAGA DURGA	4	5	5	5	5	5
85	178B1A0485	PATHI TULASI REDDY	5	4	5	5	4	4
86	178B1A0486	PATIBANDLA SIREESHA	4	5	4	4	4	5
87	178B1A0487	PITTU PAVAN KALYANI REDDY	5	5	5	5	5	5
88	178B1A0488	POTHUGANTI CHINNA SIDDAMMA	4	4	5	4	4	4
89	178B1A0489	RAMIREDDY PRAVALLIKA	5	4	5	5	5	4
90	178B1A0490	RAVELLA APARNA	5	5	5	4	4	5
91	178B1A0491	SALAVA POOJA	5	5	5	5	5	5
92	178B1A0492	SHAIK KARISHMA	4	4	5	5	4	5
93	178B1A0493	SURA KUSUMALATHA	4	5	5	4	5	4
94	178B1A0494	SYED MEHASEENA	5	5	4	5	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
95	178B1A0495	THANNEERU ROSHINI RUPA	4	5	5	4	5	5
96	178B1A0496	VEERANKI TEJASWI	5	5	5	4	5	5
97	178B1A0497	AKKALA PRAVEEN KUMAR REDDY	4	5	5	5	5	5
98	178B1A0498	BATTULA PRADEEP CHANDRA	5	4	5	5	4	4
99	178B1A0499	BEERALA RAM PAVAN KALYAN	4	5	4	4	4	5
100	178B1A04A0	CHITTELA HEMANTH KUMAR	5	4	4	4	5	5
101	178B1A04A1	DAMA RAMA KRISHNA	5	4	5	5	5	4
102	178B1A04A3	JALADANKI JAYAPRAKASH NARAYANA	5	5	5	4	4	5
103	178B1A04A4	KALAVAKURI SIVAKRISHNA	5	5	5	5	5	5
104	178B1A04A5	KOLISETTY MALLIKARJUNA	4	5	5	5	4	5
105	178B1A04A6	KOLLURI RAJA SHEKAR	4	5	5	4	5	4
106	178B1A04A7	KONKA VENKATA JAGADEESH BABU	5	4	4	5	5	5
107	178B1A04B0	NUKALAPATI CHANDRA SEKHAR	4	5	5	4	5	5
108	178B1A04B1	PAKALA NIKHIL GOPAL	5	5	5	4	5	5
109	178B1A04B2	PARUCHURI GOPI	4	5	5	5	5	5
110	178B1A04B3	PULLAGORLA NAGARAJ	5	5	5	5	4	4

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S.No	Roll Number	Name	1	2	3	4	5	6
111	178B1A04B4	SHAIK BAJI	4	5	4	4	4	5
112	178B1A04B5	TANNERU MAHESH	5	5	5	5	5	5
113	178B1A04B6	TELLAMEKALA RAJA HANUMA	4	4	5	4	4	4
114	178B1A04B7	THUMMALA VISHNU	5	4	5	5	5	4
115	178B1A04B8	UDDAGIRI NAVEEN	5	5	5	4	4	5
116	178B1A04B9	YESUPOGU VIJAY	5	5	5	5	5	5
117	168B1A0458	VINJAM RAGHAVENDRA PRASAD	4	5	4	4	4	5
118	168B1A04B4	Y VAMSI KRISHNA	5	4	5	5	5	4
			4.66	4.50	4.73	4.41	4.69	4.74
			93.22	90.00	94.64	88.21	93.75	94.82

Coordinator

PRINCIPAL
RISE KRISHNA SAI GANDHI
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S.V. HOD

HEAD OF THE DEPARTMENT
Department of E.C.E.
RISE Krishna Sai Gandhi Group
of Institutions,VALLURU,A.P.-523 272

RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

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NH-16, Valluru, Ongole, Prakasam (District)-523272
Department of Electronics and Communication Engineering

Certificate program Feedback Analysis

Topic : Certification program on" **PCB Design"**

Resource Person : **F.Daniel**
Director, center for Electronics System Design, Vijayawada

Dates : 24-09-2018 to 28-09-2018

Venue : Seminar Hall

Targeted Students : II Year students

S.No	No. of students Participated	No. of students given feedback	Feedback %
1	118	118	100%

Coordinator

Head of the Department

HEAD OF THE DEPARTMENT
Department of E.C.E.
RISE Krishna Sai Gandhi Group
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Department of Electronics and Communication Engineering

Certificate Program on PCB Design
Model Question Paper

Branch/Sem: II ECE/I SEM
Name of the Student: ROLL Number:

1.Which phenomenon is not reduced by the circuit paths of lowest impedances especially provided by power and return planes for shielding purposes?
a) Radiation
b) Convection
c) Noise
d) Crosstalk [ ]

2. High current circuits are purposely located or placed near the edge of PCB in accordance to the supply lines for _____
a) Removal of heat
b) Isolation of stray current
c) Reduction of path length
d) All of the above [ ]

3. Which among the below stated soldering methods is also renowned as 'High Frequency Resistance Soldering'?
a) Iron Soldering
b) Furnace Soldering
c) Torch Soldering
d) Electrical Soldering
[ ]

4. Which among the below mentioned approaches belongs to the category of In-circuit Testing?
a) Impedance Testing
b) Component Testing
c) Apply Signal and check output
d) All of the above [ ]

5. Which type of solderability testing is carried out for the generation of solder sample due to immersion of wire or sheet metal specimen in a bath of molten solder?
a) Solder Bath Testing
b) Meniscus Rise Testing
c) Solder Iron Testing
d) None of the above [ ]

6. What is/are the necessity/ies to provide guarding to precision differential amplifiers?
a) To increase leakage resistance
b) To reduce capacitance between signal conductors & ground
c) Both a and b
d) None of the above [ ]

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7. Which among the below mentioned assertions is not a way of cross-talk reduction while designing digital PCBs?
a) Decrease in the distance between conductors
b) Shielding of clock lines with guard strips
c) Reduction in the loop area of circuits
d) Avoid running of parallel traces for longer distances especially for asynchronous signals[ ]

8. Which among the below mentioned packages does not belong to the category of 'Small Outline Package'?
a) SO
b) SOP
c) SOT
d) SON [ ]

9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?
a) Analog side to analog ground
b) Digital side to digital ground
c) Use of separate power supply and connection of their ground leads to single point reference
d) Reduction of inductive loop area between power and return traces [ ]

10. Which among the below stated devices/equipments are preferred for elimination of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?
a) Coupling capacitor
b) Decoupling capacitor
c) Snubber circuits
d) All of the above [ ]

11. Which among the below specified condition is precise in the crosstalk verification mechanism using logic flow in opposite direction with the limit of avoiding dangerous interference in digital PCB designing? [ ]
a) $Z_{even} > Z_{odd}$
b) $Z_{odd} \geq 0.5\ Z_{even}$
c) $Z_{odd} \geq 0.8\ Z_{even}$
d) $Z_{odd} = Z_{even}$

12. Which terminology of PCB represents a thin photo-sensitive polymer by supporting photographic pattern of single traces or IC pads for etching?
a) Prepreg
b) Etching
c) Photo-resist
d) Solder mask [ ]

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13. Which problems are about to occur if PCB is not designed properly in a confined manner for digital circuits?
A. Diffraction
B. Refraction
C. Ground & Supply-line Noise
D. Electromagnetic Interference [ ]
a) A & B
b) B & C
c) C & D
d) A, B, C, D

14. Which among the following assists in obtaining the desired value of wave impedance in reflection phase while designing digital PCBs?
A. Width of signal lines
B. Distance between signal line and ground line
C. Signal Delays
D. Double Pulsing
a) A & B
b) B & C
c) C & D
d) A, B, C, D [ ]

15. What should be the resistance of 0.6 mm wide conductor with 15 cm length and 25 μm thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$(at 20° C)
a) 118.2 mΩ
b) 138.2 mΩ
c) 172.4 mΩ
d) 192.4 mΩ [ ]

16. The actual cost of PCB can be evaluated on the basis of _____
a) PCB size & material
b) Number of layers
c) Vias on PCB
d) All of the above [ ]

17. Which factors contribute to the occurrence of mechanical stress?
a) Resonance
b) Cracked Solder Joints
c) Both a and b
d) None of the above [ ]

18. Which type of PCB requires minimum soldering on component side in order to avoid replacement oriented difficulties?
a) Single-sided PCB
b) Double-sided PCB
c) Both a and b
d) None of the above [ ]

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19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?
a) Increase in self-inductance
b) Reduction in self-inductance
c) Stability in self-inductance
d) None of the above [ ]

20.During post assembly testing,it was found that a latch on of the connectors cannot be fully extended due to other components located near by.What would have prevented the situation from occurring?
a)The use of a 3D component
b) The use of a 3D component and component clearance rule
c) The use of a courtyard
d)The use of a courtyard and a component clearance rule [ ]

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ANSWERS

1.Answer: Convection

2.Answer: Removal of heat

3.Answer: Electrical Soldering

4.Answer: All of the above

5.Answer: Meniscus Rise Testing

6.Answer: Both a and b

7.Answer: Decrease in the distance between conductors

8.Answer: SON

9.Answer: Reduction of inductive loop area between power and return traces

10.Answer: Decoupling capacitor

11.Answer: $Z_{odd} \geq 0.8\ Z_{even}$

12.Answer: Photo-resist

13.Answer: C & D

14.Answer: A & B

15.Answer: 172.4 Mω

16.Answer: All of the above

17.Answer: Both a and b

18.Answer: Double-sided PCB

19.Answer: Reduction in self-inductance

20.Answer:The use of a courtyard and a component clearance rule

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Department of Electronics and Communication Engineering

Certificate Program on PCB Design
Model Question Paper

17/20

Branch/Sem: II ECE/I SEM
Name of the Student: K. Deepthi ROLL Number: 178[illegible]0416

1.Which phenomenon is not reduced by the circuit paths of lowest impedances especially provided by power and return planes for shielding purposes?
a) Radiation
b) Convection
c) Noise
d) Crosstalk
[b] ✓

2. High current circuits are purposely located or placed near the edge of PCB in accordance to the supply lines for _____
a) Removal of heat
b) Isolation of stray current
c) Reduction of path length
d) All of the above
[a] ✓

3. Which among the below stated soldering methods is also renowned as 'High Frequency Resistance Soldering'?
a) Iron Soldering
b) Furnace Soldering
c) Torch Soldering
d) Electrical Soldering
[d] ✓

4. Which among the below mentioned approaches belongs to the category of In-circuit Testing?
a) Impedance Testing
b) Component Testing
c) Apply Signal and check output
d) All of the above
[c] ✗

5. Which type of solderability testing is carried out for the generation of solder sample due to immersion of wire or sheet metal specimen in a bath of molten solder?
a) Solder Bath Testing
b) Meniscus Rise Testing
c) Solder Iron Testing
d) None of the above
[b] ✓

6. What is/are the necessity/ies to provide guarding to precision differential amplifiers?
a) To increase leakage resistance
b) To reduce capacitance between signal conductors & ground
c) Both a and b
d) None of the above
[c] ✓

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7. Which among the below mentioned assertions is not a way of cross-talk reduction while designing digital PCBs?
a) Decrease in the distance between conductors
b) Shielding of clock lines with guard strips
c) Reduction in the loop area of circuits
d) Avoid running of parallel traces for longer distances especially for asynchronous signals[O]

8. Which among the below mentioned packages does not belong to the category of 'Small Outline Package'?
a) SO
b) SOP
c) SOT
d) SON [d]

9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?
a) Analog side to analog ground
b) Digital side to digital ground
c) Use of separate power supply and connection of their ground leads to single point reference
d) Reduction of inductive loop area between power and return traces [d]

10. Which among the below stated devices/equipments are preferred for elimination of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?
a) Coupling capacitor
b) Decoupling capacitor
c) Snubber circuits
d) All of the above [b]

11. Which among the below specified condition is precise in the crosstalk verification mechanism using logic flow in opposite direction with the limit of avoiding dangerous interference in digital PCB designing? [C]
a) $Z_{even} > Z_{odd}$
b) $Z_{odd} \geq 0.5\ Z_{even}$
c) $Z_{odd} \geq 0.8\ Z_{even}$
d) $Z_{odd} = Z_{even}$

12. Which terminology of PCB represents a thin photo-sensitive polymer by supporting photographic pattern of single traces or IC pads for etching?
a) Prepreg
b) Etching
c) Photo-resist
d) Solder mask [C]

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13. Which problems are about to occur if PCB is not designed properly in a confined manner for digital circuits?
A. Diffraction
B. Refraction
C. Ground & Supply-line Noise
D. Electromagnetic Interference [c] ✓
a) A & B
b) B & C
c) C & D
d) A, B, C, D

14. Which among the following assists in obtaining the desired value of wave impedance in reflection phase while designing digital PCBs?
A. Width of signal lines
B. Distance between signal line and ground line
C. Signal Delays
D. Double Pulsing
a) A & B
b) B & C
c) C & D
d) A, B, C, D [a] ✓

15. What should be the resistance of 0.6 mm wide conductor with 15 cm length and 25 μm thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$(at 20° C)
a) 118.2 mΩ
b) 138.2 mΩ
c) 172.4 mΩ
d) 192.4 mΩ [c] ✓

16. The actual cost of PCB can be evaluated on the basis of _____
a) PCB size & material
b) Number of layers
c) Vias on PCB
d) All of the above [a] ✗

17. Which factors contribute to the occurrence of mechanical stress?
a) Resonance
b) Cracked Solder Joints
c) Both a and b
d) None of the above [d] ✗

18. Which type of PCB requires minimum soldering on component side in order to avoid replacement oriented difficulties?
a) Single-sided PCB
b) Double-sided PCB
c) Both a and b
d) None of the above [b] ✓

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19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?
a) Increase in self-inductance
b) Reduction in self-inductance
c) Stability in self-inductance
d) None of the above [a]

20.During post assembly testing,it was found that a latch on of the connectors cannot be fully extended due to other components located near by.What would have prevented the situation from occurring?
a)The use of a 3D component
b) The use of a 3D component and component clearance rule
c) The use of a courtyard
d)The use of a courtyard and a component clearance rule [b]

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Department of Electronics and Communication Engineering

Certificate Program on PCB Design
Model Question Paper

18

Branch/Sem: II ECE/I SEM
Name of the Student: perla.Venkata Sai Deepthi ROLL Number: 178B1A0233

1.Which phenomenon is not reduced by the circuit paths of lowest impedances especially provided by power and return planes for shielding purposes?
a) Radiation
b) Convection
c) Noise
d) Crosstalk
[B] ✓

2. High current circuits are purposely located or placed near the edge of PCB in accordance to the supply lines for _____
a) Removal of heat
b) Isolation of stray current
c) Reduction of path length
d) All of the above
[A] ✓

3. Which among the below stated soldering methods is also renowned as 'High Frequency Resistance Soldering'?
a) Iron Soldering
b) Furnace Soldering
c) Torch Soldering
d) Electrical Soldering
[D]

4. Which among the below mentioned approaches belongs to the category of In-circuit Testing?
a) Impedance Testing
b) Component Testing
c) Apply Signal and check output
d) All of the above
[C] ✗

5. Which type of solderability testing is carried out for the generation of solder sample due to immersion of wire or sheet metal specimen in a bath of molten solder?
a) Solder Bath Testing
b) Meniscus Rise Testing
c) Solder Iron Testing
d) None of the above
[A] ✗

6. What is/are the necessity/ies to provide guarding to precision differential amplifiers?
a) To increase leakage resistance
b) To reduce capacitance between signal conductors & ground
c) Both a and b
d) None of the above
[C] ✓

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7. Which among the below mentioned assertions is not a way of cross-talk reduction while designing digital PCBs?
a) Decrease in the distance between conductors
b) Shielding of clock lines with guard strips
c) Reduction in the loop area of circuits
d) Avoid running of parallel traces for longer distances especially for asynchronous signals[A] ✓

8. Which among the below mentioned packages does not belong to the category of 'Small Outline Package'?
a) SO
b) SOP
c) SOT
d) SON [D] ✓

9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?
a) Analog side to analog ground
b) Digital side to digital ground
c) Use of separate power supply and connection of their ground leads to single point reference
d) Reduction of inductive loop area between power and return traces [D] ✓

10. Which among the below stated devices/equipments are preferred for elimination of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?
a) Coupling capacitor
b) Decoupling capacitor
c) Snubber circuits
d) All of the above [B] ✓

11. Which among the below specified condition is precise in the crosstalk verification mechanism using logic flow in opposite direction with the limit of avoiding dangerous interference in digital PCB designing? [C] ✓
a) $Z_{even} > Z_{odd}$
b) $Z_{odd} \geq 0.5\ Z_{even}$
c) $Z_{odd} \geq 0.8\ Z_{even}$
d) $Z_{odd} = Z_{even}$

12. Which terminology of PCB represents a thin photo-sensitive polymer by supporting photographic pattern of single traces or IC pads for etching?
a) Prepreg
b) Etching
c) Photo-resist
d) Solder mask [C] ✓

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13. Which problems are about to occur if PCB is not designed properly in a confined manner for digital circuits?
A. Diffraction
B. Refraction
C. Ground & Supply-line Noise
D. Electromagnetic Interference
a) A & B
b) B & C
c) C & D
d) A, B, C, D

[C] ✓

14. Which among the following assists in obtaining the desired value of wave impedance in reflection phase while designing digital PCBs?
A. Width of signal lines
B. Distance between signal line and ground line
C. Signal Delays
D. Double Pulsing
a) A & B
b) B & C
c) C & D
d) A, B, C, D

[A] ✓

15. What should be the resistance of 0.6 mm wide conductor with 15 cm length and 25 μm thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$(at 20° C)
a) 118.2 mΩ
b) 138.2 mΩ
c) 172.4 mΩ
d) 192.4 mΩ

[C] ✓

16. The actual cost of PCB can be evaluated on the basis of _____
a) PCB size & material
b) Number of layers
c) Vias on PCB
d) All of the above

[D] ✓

17. Which factors contribute to the occurrence of mechanical stress?
a) Resonance
b) Cracked Solder Joints
c) Both a and b
d) None of the above

[C] ✓

18. Which type of PCB requires minimum soldering on component side in order to avoid replacement oriented difficulties?
a) Single-sided PCB
b) Double-sided PCB
c) Both a and b
d) None of the above

[B] ✓

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19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?
a) Increase in self-inductance
b) Reduction in self-inductance
c) Stability in self-inductance
d) None of the above [A]

20.During post assembly testing,it was found that a latch on of the connectors cannot be fully extended due to other components located near by.What would have prevented the situation from occurring?
a)The use of a 3D component
b) The use of a 3D component and component clearance rule
c) The use of a courtyard
d)The use of a courtyard and a component clearance rule [B]

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Department of Electronics and Communication Engineering

2017-2021 BATCH

Certificate Program on PCB Design Assessment Marks

A.Y : 2018-2019 **Year : II**

S. No	Reg. No	Name of the Candidate	Marks
1	178B1A0401	ANNAPAREDDY BHARATHI	18
2	178B1A0402	ATCHALA CHANDRAKALA	19
3	178B1A0403	BADUGU AKSHA TEJA	18
4	178B1A0404	BALAGANI SURYA KANTHAM	18
5	178B1A0405	BHUMA VENKATA SUNEETHA	17
6	178B1A0406	BURRA SAI LAKSHMI	18
7	178B1A0407	CHEREDDY KALPANA	16
8	178B1A0408	CHINTHAPATLA PAVITHRA	16
9	178B1A0409	CHIRITOTI LAVANYA	17
10	178B1A0410	DAMA VENKATA KEERTHANA	19
11	178B1A0411	G MANISHA	20
12	178B1A0412	GUNAPANENI VANDANA	19
13	178B1A0413	GUNDLAPALLI SAMPURNA	18
14	178B1A0414	JONNALA GADDA ALEKYA	18
15	178B1A0415	JONNALAGADDA SRUTHI SRAVYA	19
16	178B1A0416	KADIRI DEEPTHI	17
17	178B1A0417	KAKARLA YAMINI	19
18	178B1A0418	KANDEPI VENKATA SAI SRAVANI	20
19	178B1A0419	KOLAPARTI BHAVYASRI	20
20	178B1A0420	KOLLI MARLA SWETHA	16
21	178B1A0421	KOMATINENI MOUNIKA	16
22	178B1A0422	KONIDENA MANISHA	18
23	178B1A0423	LAKKU MEENAKSHI	15
24	178B1A0424	LAKSHMISETTY VYSHNAV KEERTHI	19
25	178B1A0425	MANNAM SRAVANI	18
26	178B1A0426	MANNEM YAMINI	19
27	178B1A0427	NARISINGU VASANTHI	17
28	178B1A0428	NERELLA VENKATA SUSHMA	17
29	178B1A0429	NUTHALAPATI SRILATHA	19
30	178B1A0430	NUTHALAPATI THRIVENI	18
31	178B1A0431	PABBISETTY SAI LAKSHMI VANDANA	20
32	178B1A0432	PABBISETTY VENKATA RAMYASRI	17

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S. No	Reg. No	Name of the Candidate	Marks
33	178B1A0433	PERLA VENKATA SAI DEEPTHI	18
34	178B1A0434	PURIMITLA NAGA LAKSHMI	19
35	178B1A0435	RENUMALA MOUNIKA	18
36	178B1A0436	SHAIK SAMINA	18
37	178B1A0437	SHAIK YASMIN	19
38	178B1A0438	SURA NARAYANAMMA	17
39	178B1A0439	THANIKANTI HARIKA	19
40	178B1A0440	UDARAGUDI SAILAJA	19
41	178B1A0441	YARICHARLA MOUNIKA	18
42	178B1A0442	ALLA ASHOKREDDY	17
43	178B1A0443	ALLIKEPALI SRIKANTH	18
44	178B1A0444	CHAKKA NITHISH	19
45	178B1A0445	DANNARAPU PAVAN KALYAN	18
46	178B1A0446	DODDI STEPHEN RAJ	18
47	178B1A0447	ELURI VENKATA SANJAY	17
48	178B1A0448	KOPPOLU RAMA KRISHNA	18
49	178B1A0449	KOTA BRAHMAREDDY	16
50	178B1A0450	MUVALA SAI VENKATA NAGA VINAY	16
51	178B1A0451	PABBISETTY MANOJ	17
52	178B1A0452	POLIMIREDDY MALAKONDA REDDY	19
53	178B1A0453	PONIGETI HANUMANTHA REDDY	20
54	178B1A0454	SANKARAMANCHI NAGAMANOHAR SHARMA	16
55	178B1A0455	SHAIK YASDHANI	19
56	178B1A0456	SIGHAKOLLI BALA SUBRAMANYAM	16
57	178B1A0457	SUNDARASETTY NIKHIL	20
58	178B1A0458	THOGURU PRAVEEN KUMAR	16
59	178B1A0459	THOKALA SAMSON	19
60	178B1A0460	VEMA SAI REVANTH KUMAR	18
61	178B1A0461	ADAPALA ANUSHA	19
62	178B1A0462	ALURI RAYELAMMA	18
63	178B1A0463	BATCHALI VENKATA SAI SARATH PRATYUSHA	17
64	178B1A0464	BIJJAM SRI LEENA	17
65	178B1A0465	BIRUDURAJU NAVYA SUSHMA	17
66	178B1A0466	CHINTHALA KEERTHANA	19
67	178B1A0467	DEVULAPALLI MAHALAKSHMAMMA	16
68	178B1A0468	DODDAKA NAGA DEEPTHI	18
69	178B1A0469	DONEMPUDI ANUSHA	18

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S. No	Reg. No	Name of the Candidate	Marks
70	178B1A0470	GUJJULA MAHALAKSHMI	18
71	178B1A0471	GUNJI ANUSHA	16
72	178B1A0472	KALLAGUNTA VANI VARSHITHA	19
73	178B1A0473	KARETI PRAVALLIKA	18
74	178B1A0474	KATTA HYNDAVI	19
75	178B1A0475	KELAM RAMA DEVI	18
76	178B1A0476	MADALA VENKATA SAI LAKSHMI	17
77	178B1A0477	MARELLA VENKATA SIREESHA	18
78	178B1A0478	MOLAKALAPALLI MADHAVI LATHA	17
79	178B1A0479	MONDRU MARY AMULYA	18
80	178B1A0480	MOTHUKURI ANILA	19
81	178B1A0481	MULAGANI UMA DEVI	18
82	178B1A0482	NELAMALLI SUREKHA	18
83	178B1A0483	NUKATHOTI DEENAMMA	17
84	178B1A0484	PATHAKAMURI VIJAYA NAGA DURGA	18
85	178B1A0485	PATHI TULASI REDDY	16
86	178B1A0486	PATIBANDLA SIREESHA	16
87	178B1A0487	PITTU PAVAN KALYANI REDDY	16
88	178B1A0488	POTHUGANTI CHINNA SIDDAMMA	17
89	178B1A0489	RAMIREDDY PRAVALLIKA	19
90	178B1A0490	RAVELLA APARNA	20
91	178B1A0491	SALAVA POOJA	16
92	178B1A0492	SHAIK KARISHMA	19
93	178B1A0493	SURA KUSUMALATHA	18
94	178B1A0494	SYED MEHASEENA	19
95	178B1A0495	THANNEERU ROSHINI RUPA	17
96	178B1A0496	VEERANKI TEJASWI	19
97	178B1A0497	AKKALA PRAVEEN KUMAR REDDY	16
98	178B1A0498	BATTULA PRADEEP CHANDRA	18
99	178B1A0499	BEERALA RAM PAVAN KALYAN	18
100	178B1A04A0	CHITTELA HEMANTH KUMAR	18
101	178B1A04A1	DAMA RAMA KRISHNA	15
102	178B1A04A3	JALADANKI JAYAPRAKASH NARAYANA	19
103	178B1A04A4	KALAVAKURI SIVAKRISHNA	18
104	178B1A04A5	KOLISETTY MALLIKARJUNA	19
105	178B1A04A6	KOLLURI RAJA SHEKAR	17
106	178B1A04A7	KONKA VENKATA JAGADEESH BABU	19

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NH-16, Valluru, Ongole, Prakasam (District)-523272
Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
107	178B1A04B0	NUKALAPATI CHANDRA SEKHAR	19
108	178B1A04B1	PAKALA NIKHIL GOPAL	17
109	178B1A04B2	PARUCHURI GOPI	18
110	178B1A04B3	PULLAGORLA NAGARAJ	17
111	178B1A04B4	SHAIK BAJI	18
112	178B1A04B5	TANNERU MAHESH	19
113	178B1A04B6	TELLAMEKALA RAJA HANUMA	18
114	178B1A04B7	THUMMALA VISHNU	18
115	178B1A04B8	UDDAGIRI NAVEEN	18
116	178B1A04B9	YESUPOGU VIJAY	19
117	168B1A0458	VINJAM RAGHAVENDRA PRASAD	18
118	168B1A04B4	Y VAMSI KRISHNA	19

Coordinator

HOD

HEAD OF THE DEPARTMENT
Department of E.C.E
RISE Krishna Sai Gandhi Group
of Institutions,VALLURU,A.P.-523 272

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DEPARTMENT OF ECE

[Certificate program on PCB Design

24-09-2018 to 28-09-2018]

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The Certificate Program conducted by ECE department on 24th - 28th September 2018 in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS in association with Center for Electronics System Design (CESD)

Department of Electronics & Communication Engineering

Objectives of conducting Certificate program

- To make students learn and interact with renowned industry experts.
- Make Students to receive an unparallel education on the art of **PCB Designing Certificate program** with personal one on one attention.
- To make every student an expert in designing their own **PCB board** which would be very useful for developing their own projects.

Overview about Certificate Program:

The aim of this **Certificate Program** is to make the students learn the designing and manufacturing of a printed circuit board using open source KICAD PCB design software and with various active and passive components such as Regulators, Diodes, Resistors, Capacitors, Inductors, Switches, e.t.c.

Technical Support:

The **Certificate Program** was conducted in collaboration with Center for Electronics System Design (CESD) from Vijayawada. The company has a fast growth in PCB designing. The company's director Mr. Finney Daniel accompanied with Seven Trainers attended the Certificate Program for guiding the students in learning the technologies of the PCB Design Certificate Program. They have taken about 32 hours of theoretical and practical sessions.

Department of ECE:

Department of ECE has taken the opportunity to conduct the in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS. As the theme of the Certificate Program is the core for the department, it's a nice opportunity for the students to learn the technology and to implement that practically.

Technical Report on Certificate Program:

The Technical team of Center for Electronics System Design (CESD) has described the entire designing process in a step by step procedure.

1. **Basic PCB Concepts**
   First of all they have given the concepts which will be very helpful for designing the PCB practically, using some power point presentations. In this theoretical explanation part they have explained about the KI-CAD software and the use of software for further practical implementation in designing the PCB. They have also

Principal
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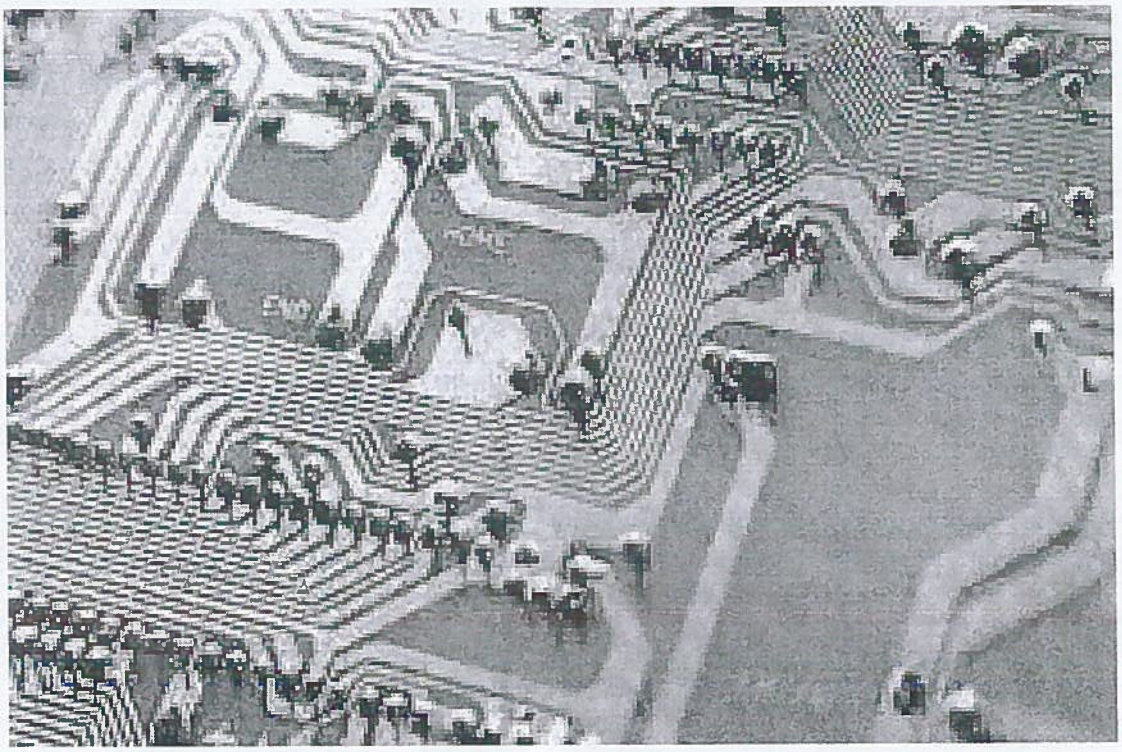
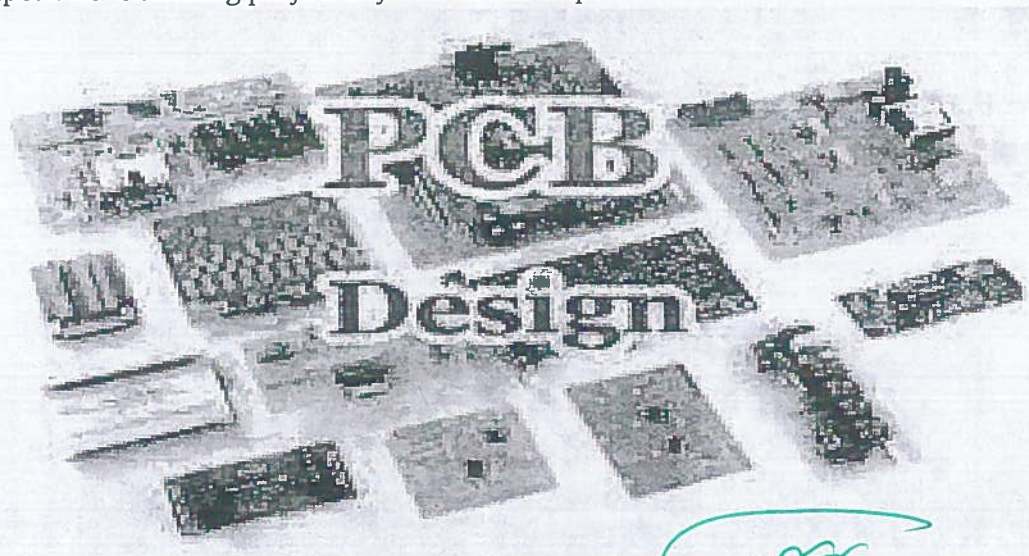
given a briefing about active and passive electronic components which they will be using in a PCB.



2. **Editing and Routing**

Editing and Routing is the basic step and it is one of the important step for designing a PCB. Editing and Routing gives the circuit layout from one component to the other components. Soldering plays a key role in this step.



3. **Creation of Library and Components & Report Generation**
   This is a step done using KI-CAD tools. In this step the components in the circuit and the respective libraries are selected in this software. So that the required circuit will be designed in the software and a print of the same will be taken on a sheet. The same print will be useful for the further process.

4. **Toner Transfer Method**
   This is the step where the designed circuit will be pasted on the wafer and this will be passed through a temperature of about 160 to 180 degrees so that the tracks of the circuit will be remained on the wafer. The tracks will be a conductive type.
5. **Drilling Technique**
   The board will be drilled with holes where the components have to be placed; the holes will be drilled in the board depending on the terminals available for the components in the design. The hole should be in the size so that the terminal has to be freely placed in the hole.
6. **Soldering Technique**
   The components that are placed in the board should be soldered to the track so that the circuit is connected as per the design. After this step the engraved PCB will be ready to use.

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The Department conducted test on PCB Design for Electronic components and all project models are exhibited in the respected department

Student Response

Almost 118 students had taken part in the Certificate Program. All the students responded that they have learned and had hands on experience in designing a PCB. They are very excited in participation in this Certificate Program and requested for more Certificate Program in similar way so that they can simultaneously gain the practical knowledge.

Distribution of Certificates

At the last day question answer session and certificate distribution function started on 4:30 PM. Feedbacks regarding workshop are provided by various students.

All the students were awarded with a participation certificate from the company Center for Electronics System Design(CESD). Principal Dr.K.V.Subrahmanyam garu awarded the certificates to all the students by hand. He personally congratulated every student for participating in the event and making it successful.

Vote of Thanks

Mr.S V Ravi Kumar beloved HOD of ECE Department thanked every student for their active participation and interest in participating in the Certificate Program and mentioned about the activities conducted in the college by the department. He promised that department will continue its assistance in conducting these sorts of Certificate Programs and seminars in future.

He thanked the technical support given by **Center for Electronics System Design (CESD).** He personally felt very happy for the response of the company and satisfied with the way they conducted the Certificate Program.

He mentioned about the marvelous support given by the Principal Dr.K.V.Subrahmanyam garu to the department in conducting these Certificate Program. He also thanked for the personal interest taken by him in encouraging the department in all aspects.

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Department of Electronics and Communication Engineering

Date: 28-09-2018.

CLOSING REPORT

To,
The Principal,
RISE Krishna Sai Gandhi Group of Institutions.

As per the approved schedule, the ECE department has conducted a Certificate Program on **"PCB Design"** at ECE Seminar hall from 24-09-2018 to 28-09-2018. 118 students of II ECE have participated in this program. Sri **F.Daniel,** Director, Center for Electronics Systems Design (CESD), Vijayawada, AP, acted as the resource person for this program.

Main issues addressed:

1. Basic PCB Concepts
2. Editing and Routing
3. Creation of Library and Components & Report Generation
4. Toner Transfer Method
5. Drilling Technique
6. Soldering Technique

We are expecting your support in future also. Thanking you sir,

Yours faithfully,

Coordinator

HOD

HEAD OF THE DEPARTMENT
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