Department of Electronics and Communication Engineering



Certificate Program

"PCB Design "

Date: 21<sup>th</sup>to 25<sup>th</sup> Feb - 2022

Finney Daniel

Dirctor, center for electronics system design Vijayawada

RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

VALLURU:: ONGOLE.



(Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada) NH-16, Valluru, Ongole, Prakasam (District)-523272

Valluru,

Date: 28-01-2022

To

F.Daniel, Dirctor, Center for Electronics System Design, Vijayawada.

Dear Sir,

Subject: Inviting for Certificate program - Reg.

Greetings from RISE Krishna Sai Gandhi Group of Institutions, Ongole

VALLURU:: UNGOLE.

As per the discussion with Dr.K.V.Subrahmanyam, Principal, of our Institute, I hereby take this opportunity to invite you to conduct the Certificate program on **PCB Design** "From 21-02-2022 to 25-02-2022.

You are requested to interact and provide guidance to our II B.Tech students, who are looking forward to their bright career ahead. I will feel honored by your gracious presence at our organization. I believe that your lecture will help our students and faculty members to explore knowledge.

Thanking you in anticipation.

Yours sincerely,

PRINCIPAL

RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

VALLURU: ONGOLE.

## **Finney Daniel**

Managing Director
Center for Electronics System Design

#### **Personal Summary**

Finney Daniel has a record of organizing Institutional Industry oriented up-gradation programs for undergraduates. Experienced in delivering recent trend technologies to the personnel in vivid methodologies. Providing a lawn of possibilities in the specified area which strengthen the personnel in growing the skills required for their success in the present day competence. He has experience as a guest lecturer, assistant professor and a research fellow. His main interest in this has been to prove the potential and ability of the personnel.

#### **Professional Summary**

- Delivered services as Guest Lecturer for VLSI in Andhra University College of Engineering.
- Worked as Assistant Professor in couple of Engineering Colleges.
- As Junior Research Fellow in Defence Research & Development Laboratory.

#### Areas of Expertise

- **Product Development:** Evolving modules that enable a final product meeting the End- User requirements and facilitate easy utility of the product
- Project Management: Maintaining strategic planning and supporting the team in delivering Robust Models by providing employ friendly platform.
- Organizing Training Sessions: Planned tabulation for training and hands on expertise for the personnel under training.

#### Professional Skills and Competencies

- Strong knowledge on Software tools like QUARTUS, Xilinx, Cadence, Tanner- EDA, Mentor-Graphics required for VLSI.
- Good knowledge on hardware design and development includes familiarity in Embedded System tools and PCB design tools like MPLAB Xpress IDE, KEIL, Micro-c, ZUKEN- Cadstar, Eagle, Express-PCB.

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#### **Key Roles**

- Academic Director for KR's Educational Society.
- Coordinator for Technical Symposium in Holy Mary Group of Institutions.
- Organized Workshops on Verilog, PCB Design, Prototyping, Embedded Systems, Product Design and Development.

#### Qualification

- Master of Technology in VLSI-System Design from JNTU-Kakinda.
- PG Diploma in Electronic Product Design from Electronics System Design and Manufacturing (ESDM, Govt. of India).
- Graduation in Electronics & Communication Engineering from CJITS, JNTU- Hyderabad.
- Graduation in Bachelor of Science in Mathematics from Andhra University.

#### Personal Details

- Born on 21<sup>st</sup> June 1987 in Visakhapatnam.
- Indian citizen and can speak Hindi, English, Telugu.

References - Available on Request.

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## PROPOSAL FORM

SUB: Certificate program - Program.

## TO THE SECRETARY/CORRESPONDENT THROUGH PRINCIPAL FOR KIND APPROVAL

1	NAME OF THE INSTITUTION	Rise Krishna Sai Gandhi Group of Institutions
2	NAME OF THE DEPARTMENT	Electronics & Communication Engineering
3	TITLE OF THE PROGRAMME	Certificate program
4	NAME OF THE PROGRAMME	Certificate program on "PCB Design for Electronic Designs"
5	OBJECTIVE OF THE PROGRAMME	To bring the exposure in the PCB Design.
6	DETAILS OF RESOURCE PERSON(S)& CV ATTACHED.	Finney Daniel Director, center for electronics system design Vijayawada.
7	PROPOSED DATE(S)/ACADEMIC YEAR	21-02-2022 to 25-02-2022
8	DURATION OF THE PROGRAMME	FIVE DAY
9	VENUE	Seminar Hall
10	TARGETS	II ECE students
11	No. OF PARTICIPANTS	113 Students
12	REGISTRATION FEE	Free
13	NAME OF PROGRAMME CO ORDINATOR(S)	Mr. K.Nagahanuma Chari
14	NAME OF THE STUDENTS COORDINATOR(S)	1.Ms. Valiveti Thanuja (208B1A0423) 2.Mr. Poka Mahesh Babu (208B1A0492)

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Department of Electronics and Communication Engineering

15	SOURCE OF FUND IDENTIFIED	Management
16	MANAGEMENT CONTRIBUTION REQUIRED	YES
17	PROPOSAL PREPARED BY	Mr.K.Nagahanuma Chari (CO-ORDINATOR)

Coordinator

HOD
HEAD OF THE DEPARTMENT
Department of E.C.E.
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P. 523 272

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Valluru,

Date: 18-02-2022.

#### CIRCULAR

This is to inform II B.Tech students and faculty that there will be a 5-Day Certificate program on "PCB Design" from 21-02-2022 to 25-02-2022 by F.Daniel, Director, Center for Electronics System Design, Vijayawada.

Copy to:

Principal

Staff Circular

Students of ECE II year

ECE Department Notice Boards

S.N. Shop

HEAD OF THE DEPARTMENT
Department of E.C.E
RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P.-523 272

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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

## Certificate Program on "PCB Design"

Date: 21<sup>th</sup>to 25<sup>th</sup>Feb 2022

## SCHEDULE FROM 21-02-2022 TO 25-02-2022

S. No	Program List	Timing			
		From	То		
	DAY - 01 (21-02-20	022)			
1	Program started	09.00 AM			
2	Lamp lighting	09.00 AM	09.10 AM		
3	Principal speech	09.10 AM	09.25 AM		
4	HOD Introduction about PCB Design	09.25 AM	09.35 AM		
5	Tea Break	09.35 AM	10.00 AM		
6	Introduction about PCB concepts	10.00 AM	01.00 PM		
7	Lunch Break	01.00 PM	01.45 PM		
8	KI-CAD Software Practical Section	01.45 PM	05.00 PM		
	DAY - 02 (22-02-2	022)			
9	Concepts of PCB Designing, PCB	09.00 AM	12.15 PM		
	Materials, Layers				
10	Lunch Break	12.15 PM	01.00 PM		
11	Multilayer Concepts	01.00 PM	05.00 PM		
	DAY - 03 (23-02-2				
12	PADSTACK	09.00 AM	12.15 PM		
13	Lunch Break	12.15 PM	01.00 PM		
14	Schematic entry KI-CAD tools	01.00 PM	05.00 PM		
	DAY - 04 (24-02-2	.022)			
15	Drawing a schematic FLAT	09.00 AM	12.15 PM		
16	Lunch Break	12.15 PM	01.00 PM		
17	BOM. Net list generation	01.00 PM	05.00 PM		
	DAY - 05 (25-02-2	2022)			
18	Designing Boards	09.00 AM	12.15 PM		
19	Lunch Break	12.15 PM	01.00 PM		
20	Drawing a schematic HIERARCHICAL Design	01.00 PM	04.15 PM		
21	Certificate Program Exam	04.15 PM	04.45 PM		
22	Vote of Thanks	04.45 PM	05.00 PM		

Coordinator

RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS. VALLURU:: ONGOLE.



### RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Student: Shail Codishma
Roll No

Roll No : 208 BI AD 417
Topic: Certificate Program on "PCB Design"

Date: 25-02-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?	1				
2.	Is the certification program well planned or not?	اسرا				
3	Lecture makes objectives clear?		1			
4	Lecture speaks clearly and audibly?	1				
5	Lecture explains with exaples clearly?	VAII.	-	ingue:		
6	Is you are doubts clarified or not?	William Committee of the Committee of th	~			

5-Excellent

4-Good

3-Average 2-Poor

1- No comment

Sh. lasishma

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## RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT TELECTRONICS AND COMMUNICATION ENGINEERING

## Student Feedback Form

Name of the Student: Madam malathi

Roll No : 2088 | Aouly Topic : Certificate Program on "PCB Design"

Copic: Certificate Program on "PCB Design" Date: 25-02-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?	4				
2	Is the certification program well planned or not?	<u></u>				
, 3	Lecture makes objectives clear?	M				
4	Lecture speaks clearly and audibly?		<u></u>			
5	Lecture explains with exaples clearly?		L-M			
6	Is you are doubts clarified or not?		~			

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

M, malash; Student Signature

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### RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Student: GOD Sepati Manjula
Roll No : 308 Bl Apulo 8
Topic: Certificate Program on "PCB Design"

Date: 25-02-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?	-				
2	Is the certification program well planned or not?	~				
3	Lecture makes objectives clear?					
4	Lecture speaks clearly and audibly?		<u></u>			
5	Lecture explains with exaples clearly?					
6	Is you are doubts clarified or not?	~				

5-Excellent

4-Good

3-Average 2-Poor

1- No comment

Student Signature

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#### RISE KKISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT C SLECTRONICS AND COMMUNICATION ENGINE ING

**Student Feedback Form** 

Name of the Student: Malclana waveena

Roll No : 208 Bl A0 U3
Topic : Certificate Program on "PCB Design"

Date: 25-02-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?		<u></u>			
2	Is the certification program well planned or not?					
3	Lecture makes objectives clear?	35 A	V			
4	Lecture speaks clearly and audibly?		L			
5	Lecture explains with exaples clearly?	1				
6	Is you are doubts clarified or not?	L				

5-Excellent

4-Good

3-Average 2-Poor

1- No comment

M, Weny Student Signature

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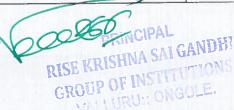
## RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING CERTIFICATE PROGRAM FEEDBACK ANALYSIS

A.Y: 2021-2022

Year: II B. Tech ECE

Date: 25-02-2022

S.No	Roll Number	Name	1	2	3	4	5	6
1	208B1A0401	ALLIBOYINA JHANSI LAKSHMI	4	5	5	5	5	5
2	208B1A0402	AMARTHALURI PRASANTHI	5	5	5	5	4	5
3	208B1A0403	BANDARU REETHIKA	4	5	4	5	5	5
4	208B1A0404	BANDARU SAI PRASANNA LAKSHMI	5	5	4	5	5	4
5	208B1A0405	CHODA AKHILA	5	5	5	5	5	5
6	208B1A0406	GOGULA NAGA MOUNIKA	5	5	4	5	4	4
7	208B1A0407	GONUGUNTLA THANMAI	4	5	4	5	5	5
8	208B1A0408	GORREPATI MANJULA	5	5	5	5	4	5
9	208B1A0409	GUNDLATHOTI ANJALI	4	5	4	5	5	5
10	208B1A0410	ILA THIRUPATHAMMA	5	5	4	4	5	5
11	208B1A0411	KASIREDDY UMA	5	5	4	4	5	4
12	208B1A0412	KONISAM TIRUPATHAMMA	5	5	4	5	4	4
13	208B1A0413	MAKKENA NAVEENA	4	4	4	5	5	5
14	208B1A0414	MARAM MALATHI	5	4	4	4	5	4
15	208B1A0415	MITHUKULLA AMULYA	4	5	4	5	5	4
16	208B1A0416	PULICHERLA ADILAKSHMI	5	4	5	5	5	4
17	208B1A0417	SHAIK KARISHMA	5	5	4	5	4	4



S.No	Roll Number	Name	1	2	3	4	5	6
18	208B1A0419	SWARNA GAYATHRI	5	4	4	4	5	4
19	208B1A0420	TENALI SAI SUPRAJA	۵	5	4	5	5	4
20	208B1A0421	TUMMAPUDI VENKATA LAKSHMI AKHILA	5	5	. 5	4	4	4
21	208B1A0422	UTUKURI LAKSHMIPRASANNA	4	5	4	5	5	5
22	208B1A0423	VALIVETI THANUJA	۷	4	4	5	5	4
23	208B1A0424	VALLEPU ANUSHA	5	4	4	5	5	4
24	208B1A0425	YANNAM NAGA MALLESWARI	4	5	5	4	4	4
25	208B1A0426	YELCHURI LAKSHMI PRIYA	4	5	5	5	5	5
26	208B1A0427	ASUPALLI SIVA REDDY	4	4	5	4	4	4
27	208B1A0428	BOGISETTY SURYA PRAKASH	5	4	5	5	5	4
28	208B1A0430	GATTUPALLI VENKATA SAI KRISHNA SATHVIK	5	4	5	5	5	4
29	208B1A0431	GOGULA SUNIL SANDESH	۷	4	4	5	4	5
30	208B1A0433	GUDIPATI VENKATA RAKESH	5	5	5	4	5	5
31	208B1A0434	MANCHALA VENKATESWARLU	4	5	5	5	5	5
32	208B1A0435	MARAMREDDY VISHNU VARDHAN REDDY	5	5	5	4	5	5
33	208B1A0436	MUNNANGI ADARSH	2	5	5	4	5	5
34	208B1A0437	MYPATI ASHOK KUMAR	5	4	5	5	4	4
35	208B1A0438	PALLABOTHULA PRASANTH	4	5	5	4	5	5
36	208B1A0439	PATHAKAMURI LOKESH	5	4	5	5	5	5
37	208B1A0440	POTTURI VENKAT KARTHIKEYA	7	5	5	4	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
38	208B1A0441	PULLELA VENKATA SAI KUMAR	5	5	5	4	5	5
39	208B1A0442	PURANAM MANIKANTA	5	5	4	4	5	5
40	208B1A0443	SAPPARAPU SYAM	5	5	5	5	5	5
41	208B1A0444	SHAIK TIPPU FIROZ	4	5	5	4	5	5
42	208B1A0445	SINGAMSETTY VENKATA SAI SUBHASH	5	5	5	4	5	5
43	208B1A0446	SINGARAJU ARAVIND	4	4	5	4	5	5
44	208B1A0447	SYED JILANI	5	5	5	5	4	4
45	208B1A0448	VARIKUTI ANIL REDDY	5	5	5	5	5	5
46	208B1A0449	VEMULA BALAKRISHNA	5	4	4	5	5	5
47	208B1A0450	YALLAVULA MANOHAR REDDY	4	5	5	5	4	5
48	208B1A0451	AMARA LAKSHMI MOUNIKA	5	5	5	5	5	5
49	208B1A0452	BHAVANAM KEERTHI	5	5	4	4	5	5
50	208B1A0453	BHUPATHI ANUSHA	5	5	5	5	5	5
51	208B1A0454	BISAI SIREESHA	5	4	5	5	4	4
52	208B1A0455	BOLLA MAMATHA	4	5	5	5	5	5
53	208B1A0456	BUSI JYOSHNA	5	5	5	5	4	5
54	208B1A0458	DESAM NAGAMANI	5	4	4	5	5	4
55	208B1A0459	DEVARAPALLI HARSHITHA	4	5	5	5	5	5
56	208B1A0460	IDAMAKANTI SRAVANI	5	5	5	5	4	5
57	208B1A0461	KASIREDDY VASUNDHARA	5	5	4	5	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
58	208B1A0462	KOLIKI SIRISHA	5	5	5	5	4	5
59	208B1A0463	MUPPARAJU SRAVANI	4	5	5	4	4	4
60	208B1A0464	PALAGUMMI GNANA VENKATA RAJANI	5	5	5	4	4	5
61	208B1A0465	PALLAPU AMANI	4	5	5	5	5	5
62	208B1A0466	PERISOMULA VASAVI HANVITHA	5	5	4	5	4	4
63	208B1A0467	POTHURAJU LAKSHMI PRATHYUSHA	5	5	5	5	5	5
64	208B1A0468	VALLEPU NAGASIVA	4	5	4	5	5	5
65	208B1A0469	ALUGUNDLA VENKATA SIVA REDDY	5	5	5	4	5	5
66	208B1A0470	AMARTHALURI NAGA VAMSI	5	4	5	5	5	5
67	208B1A0471	AMBATI MANOHAR SAI	5	4	4	5	5	4
68	208B1A0472	BADITHALA SAI VAMSI KRISHNA	4	5	5	4	5	5
69	208B1A0473	BASAM HEMANTH KUMAR	4	4	5	5	4	4
70	208B1A0474	BHIMISETTY SUDHEER BABU	5	5	4	5	4	5
71	208B1A0475	CHIMMIRI BALAJI	4	4	5	5	5	5
72	208B1A0476	CHINTAM KUMAR	4	4	5	5	4	4
73	208B1A0477	CHUNDURI VAMSI	5	4	4	4	5	5
74	208B1A0478	DASARI VENKATA RISHI RAMANAND	4	4	5	5	4	5
75	208B1A0479	G S RANJITH KUMAR REDDY	4	5	5	4	5	4
76	208B1A0480	GUNDEBOMMA SIVA SANKAR PRASAD	4	4	4	5	5	5
77	208B1A0481	GUNIMINI SAI KIRAN	4	5	5	5	5	5



S.No	Roll Number	Name	1	2	3	4	5	6
78	208B1A0482	KATTA VASU	4	4	5	4	5	4
79	208B1A0483	KONGARA KARTHIK	4	5	5	5	5	5
80	208B1A0484	KONKA NARENDRA	4	4	5	5	5	5
81	208B1A0485	KUNCHALA SRIKANTH	5	5	4	4	5	4
82	208B1A0486	KUNCHALA TARUN	4	5	5	4	5	5
83	208B1A0487	KUNCHELA SRI HARI	4	5	4	5	5	5
84	208B1A0488	MADALA VENKATESWARLU	4	4	5	5	5	5
85	208B1A0489	METTA PAVANKALYAN	5	5	5	5	5	5
86	208B1A0491	PATAN SURAJ KHAN	4	5	4	5	5	4
87	208B1A0492	POKA MAHESH BABU	4	4	5	4	5	5
88	208B1A0493	PUSALA RAMAN TARUN TEJA	4	4	5	4	4	4
89	208B1A0494	PUTTA VENKATA THARUN KUMAR	5	4	4	4	4	5
90	208B1A0495	SRUNGARAPU VENKATA SAI AKASH	5	5	5	5	5	5
91	208B1A0496	SUNKARI NARASIMHA NAIDU	5	4	5	4	4	4
92	208B1A0497	TANIKONDA GANESH	5	4	5	5	5	5
93	208B1A0498	THAPPETA SAMPATH KUMAR	5	5	4	4	4	5
94	208B1A0499	THULASI DINESH KUMAR	4	4	5	4	5	4
95	208B1A04A0	UDAYAGIRI HARSHITH	5	4	5	4	5	5
96	208B1A04A1	UPPU DINESH	5	4	5	4	5	5
97	208B1A04A2	YADALA MANI KANTA	5	5	4	4	4	5

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S.No	Roll Number	Name	1	2	3	4	5	6
98	208B1A04A3	YENUBARI PRAMOD SAGAR	5	5	4	5	4	4
99	208B1A04A4	NAGINENI RAMUDU	5	4	4	4	5	5
100	218B5A0401	GOURAVARAPU HARISHA	5	5	4	5	-5	5
101	218B5A0402	NALAMOTHU KALYANI	5	4	5	4	4	5
102	218B5A0403	PURINI SINDHUJA	5	5	5	4	4	4
103	218B5A0404	PYDALA PRANAVI	5	4	5	4	4	4
104	218B5A0405	SODA DIVYA	4	5	5	4	4	4
105	218B5A0406	TIPPABATHINA PRASANNA LAKSHMI	5	4	5	4	5	4
106	218B5A0407	VARIKALLU PREMANKITHA	5	4	4	5	5	5
107	218B5A0408	YEDLURI NEERAJA	5	4	5	5	5	5
108	218B5A0409	BADAM ASHOK REDDY	5	5	5	5	5	5
109	218B5A0410	DAADI YASWANTH SRINIVAS	5	4	4	4	4	5
110	218B5A0411	ETIPOGU DEVID	5	5	5	5	5	5
111	218B5A0412	GUMMOJI VENKATA LOKNATH	4	5	4	5	4	4
112	218B5A0413	KAMJULA YASHWANTH RAGHAVA REDDY	5	4	4	4	5	5 .
113	218B5A0414	PAPPU BHANU PRAKASH	5	5	5	5	5	5
	HEND BURNE		4.60	4.47	4.62	4.44	4.65	4.68
			92.00	89.41	92.35	88.82	92.94	93.53

Coordinator

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HEAD OF THE DEPARTMENT
Department of E.C.E

RISE Krishna Sai Gandhi Group
of Institutions, VALLURU, A.P. 523 272



(Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada)
NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

## Certificate program Feedback Analysis

Topic

: Certification program on" PCB Design"

Resource Person

: F.Daniel

Director, center for Electronics System Design, Vijayawada

Dates

: 21-02-2022 to 25-02-2022

Venue

: Seminar Hall

Targeted Students

: II Year students

S.No	No. of students Participated	No. of students given feedback	Feedback %
1	113	113	100%

Coordinator

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S.V. DOD & S

HEAD OF THE DEPARTMENT Department of E.C.E. RISE Krishna Sai Gandhi Group



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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

### Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM Name of the Student:	ROLL Number:
1. Which phenomenon is not reduced by the circuit path provided by power and return planes for shielding purp	as of lowest impedances especially oses?
a) Radiation	
b) Convection	
c) Noise	
d) Crosstalk	
2. Which among the below stated soldering methods is	also renowned as riigh riequency
Resistance Soldering'?	
a) Iron Soldering	
b) Furnace Soldering	
c) Torch Soldering	
<ul><li>d) Electrical Soldering</li><li>3. Which among the below mentioned approaches belo</li></ul>	
	migs to the category of m-encur
Testing? a) Impedance Testing	
b) Component Testing	
c) Apply Signal and check output	
d) All of the above	
4. What is/are the necessity/ies to provide guarding to	precision differential amplifiers?
a) To increase leakage resistance	,
b) To reduce capacitance between signal conductors &	ground
c) Both a and b	8
d) None of the above	
5. When a pentavalent impurity is added to a pure sem	
a) An insulator	
b) An intrinsic semiconductor	
c) p-type semiconductor	
d) n-type semiconductor	
6. High current circuits are purposely located or placed	d near the edge of PCB in
accordance to the supply lines for	
a) Removal of heat	
b) Isolation of stray current	
c) Reduction of path length	
d) All of the above	[]

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7. Which among the below mentioned packages does not belong to the category of 'Sn	nall
Outline Package'?	
a) SO	
b) SOP	
c) SOT	1
d) SON	
8. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?	
a) Increase in self-inductance b) Reduction in self-inductance	
c) Stability in self-inductance	
d) None of the above	1
9. Which among the below specified assertions is not a grounding consideration	,
associated with ADC as well as DAC?	
a) Analog side to analog ground	
b) Digital side to digital ground	
c) Use of separate power supply and connection of their ground leads to single point	
reference	
d) Reduction of inductive loop area between power and return traces	]
10. Which among the below stated devices/equipments are preferred for elimination	
of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?	
a) Coupling capacitor	
b) Decoupling capacitor	
c) Snubber circuits	
d) All of the above	_
11. Which among the below specified condition is precise in the crosstalk verification	n
mechanism using logic flow in opposite direction with the limit of avoiding dangerou	
interference in digital PCB designing?	]
a) $Z_{\text{even}} > Z_{\text{odd}}$	
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$	
c) $Z_{\text{odd}} \ge 0.8 Z_{\text{even}}$	
d) $Z_{\text{odd}} = Z_{\text{even}}$	
12. Which terminology of PCB represents a thin photo-sensitive polymer by supporti	ing
photographic pattern of single traces or IC pads for etching?	
a) Prepreg	
b) Etching	
c) Photo-resist	1
d) Solder mask	]
13. Which problems are about to occur if PCB is not designed properly in a confined manner for digital circuits?	
A. Diffraction	
B. Refraction	
C. Ground & Supply-line Noise	
D. Electromagnetic Interference	1
a) A & B	

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b) B & C	
c) C & D	
d) A, B, C, D	
14. Which type of solderability testing is carried out for the generation of solder	sample
due to immersion of wire or sheet metal specimen in a bath of molten solder?	
a) Solder Bath Testing	
b) Meniscus Rise Testing	
c) Solder Iron Testing	
d) None of the above	[ ]
15. Which among the following assists in obtaining the desired value of wave in	npedance
in reflection phase while designing digital PCBs?	
A. Width of signal lines	
B. Distance between signal line and ground line	
C. Signal Delays	
D. Double Pulsing	
a) A & B	
b) B & C	
c) C & D	
d) A, B, C, D	
16. What should be the resistance of 0.6 mm wide conductor with 15 cm length	and 25
$\mu$ m thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6} (at 20^{\circ} C)$	
a) 118.2 m $\Omega$	
b) 138.2 mΩ	
c) 172.4 mΩ	rì
d) 192.4 m $\Omega$	[ ]
17. The actual cost of PCB can be evaluated on the basis of	
a) PCB size & material	
b) Number of layers	
c) Vias on PCB	r 1
d) All of the above	[]
18. Which factors contribute to the occurrence of mechanical stress?	
a) Resonance	
b) Cracked Solder Joints	
c) Both a and b	гэ
d) None of the above	[ ]
19. Which type of PCB requires minimum soldering on component side in ord	er to avoi
replacement oriented difficulties?	
a) Single-sided PCB	
b) Double-sided PCB	
c) Both a and b	F 3
d) None of the above	

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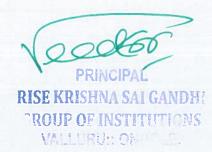
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- 20. Addition of pentavalent impurity to a semiconductor creates many .......
- a) Free electrons
- b) Holes
- c) Valence electrons
- d) Bound electrons





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#### **ANSWERS**

1. Answer: Convection

2. Answer: Electrical Soldering

3. Answer: All of the above

4. Answer: Both a and b

5. Answer: n-type semiconductor

6. Answer: Removal of heat

7. Answer: SON

8. Answer: Reduction in self-inductance

9. Answer: Reduction of inductive loop area between power and return traces

10. Answer: Decoupling capacitor

11. Answer:  $Z_{odd} \ge 0.8 Z_{even}$ 

12. Answer: Photo-resist

13.Answer: C & D

14. Answer: Meniscus Rise Testing

15.Answer: A & B

16.Answer: 172.4 Mω

17. Answer: All of the above

18. Answer: Both a and b

19 Answer: Double-sided PCB

20. Answer: Free electrons

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Department of Electronics and Communication Engineering

Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM Name of the Student: BANCOLU	Reethilca	ROLL Number: 208BIA	ю403
1. Which phenomenon is not reduced by provided by power and return planes fo a) Radiation b) Convection	the circuit paths of r shielding purpose	f lowest impedances especial! s?	ly
<ul><li>c) Noise</li><li>d) Crosstalk</li><li>2. Which among the below stated solder</li><li>Resistance Soldering'?</li><li>a) Iron Soldering</li></ul>	ering methods is also	[ <b>්</b> o renowned as 'High Frequen	cyl
<ul><li>b) Furnace Soldering</li><li>c) Torch Soldering</li><li>d) Electrical Soldering</li><li>3. Which among the below mentioned</li></ul>	approaches belongs	[d] s to the category of In-circuit	V
Testing? a) Impedance Testing b) Component Testing			. (
<ul><li>c) Apply Signal and check output</li><li>d) All of the above</li><li>4. What is/are the necessity/ies to prov</li><li>a) To increase leakage resistance</li></ul>	ide guarding to pred	[d] cision differential amplifiers?	
<ul><li>b) To reduce capacitance between sign</li><li>c) Both a and b</li><li>d) None of the above</li><li>5. When a pentavalent impurity is added</li></ul>		[C]	5
<ul> <li>a) An insulator</li> <li>b) An intrinsic semiconductor</li> <li>c) p-type semiconductor</li> <li>d) n-type semiconductor</li> <li>6. High current circuits are purposely</li> </ul>	located or placed ne	[d]	V
accordance to the supply lines for a) Removal of heat b) Isolation of stray current c) Reduction of path length			/
d) All of the above		[0]	$\vee$

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7. Which among the below mentioned packages does not belong to the category of 'Sr	nal	1
Outline Package'?		
a) SO		
b) SOP		
c) SOT	7	1
d) SON	] 1	
8. What effects can be observed if the separate power and ground planes are provided		
with large conducting surfaces for better decoupling in PCB layouts?		
a) Increase in self-inductance		
b) Reduction in self-inductance		
c) Stability in self-inductance	1	
d) None of the above	1	
9. Which among the below specified assertions is not a grounding consideration		
associated with ADC as well as DAC?		
a) Analog side to analog ground		
b) Digital side to digital ground		
c) Use of separate power supply and connection of their ground leads to single point		
reference d) Reduction of inductive loop area between power and return traces	1	-
	J	V
10. Which among the below stated devices/equipments are preferred for elimination		
of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?		
a) Coupling capacitor		
b) Decoupling capacitor		
c) Snubber circuits	7	1
d) All of the above 11. Which among the below specified condition is precise in the crosstalk verification	<i>_1</i> 1	
mechanism using logic flow in opposite direction with the limit of avoiding dangerou	2	
interference in digital PCB designing?	1	1
a) $Z_{\text{even}} > Z_{\text{odd}}$	1	V
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$		
c) $Z_{\text{odd}} \ge 0.8 Z_{\text{even}}$		
d) $Z_{\text{odd}} = Z_{\text{even}}$		
12. Which terminology of PCB represents a thin photo-sensitive polymer by support	ng	
photographic pattern of single traces or IC pads for etching?		
a) Prepreg		
b) Etching		
c) Photo-resist		
d) Solder mask	2]	. /
13. Which problems are about to occur if PCB is not designed properly in a confined	-	V
manner for digital circuits?		
A. Diffraction		
B. Refraction		
C. Ground & Supply-line Noise		1
D. Electromagnetic Interference	a	1/
a) A & B		
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b) B & C		
c) C & D		
d) A, B, C, D		
14. Which type of solderability testing is carried out for the generation of solder sa	imple	
due to immersion of wire or sheet metal specimen in a bath of molten solder?		
a) Solder Bath Testing		
b) Meniscus Rise Testing		
c) Solder Iron Testing		
d) None of the above 15. Which among the following assists in obtaining the desired value of wave important in reflection phase while designing digital PCBs?		X
15. Which among the following assists in obtaining the desired value of wave imp	edanc	e/
in reflection phase while designing digital PCBs?		
A. Width of signal lines		
B. Distance between signal line and ground line		
C. Signal Delays		
D. Double Pulsing		
a) A & B		
b) B & C		
c) C & D	1.	,
d) A, B, C, D	[h]	X
d) A, B, C, D  16. What should be the resistance of 0.6 mm wide conductor with 15 cm length at thickness of standard copper foil? (Assume o = 1.7241 x 10 <sup>-6</sup> (at 20° C)	nd 25	
$\mu$ m thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$ (at 20° C)		
a) 118.2 mΩ		
b) 138.2 mΩ		
c) 172.4 m $\Omega$	1.	
d) 192.4 m $\Omega$	[d]	V
17. The actual cost of PCB can be evaluated on the basis of		
a) PCB size & material		
b) Number of layers		
c) Vias on PCB		-
d) All of the above	[d]	/
18. Which factors contribute to the occurrence of mechanical stress?		
a) Resonance		
b) Cracked Solder Joints		
c) Both a and b		/
d) None of the above	[C]	
19. Which type of PCB requires minimum soldering on component side in order	to avo	id
replacement oriented difficulties?		
a) Single-sided PCB		
b) Double-sided PCB		/
c) Both a and b	- 1	1/
d) None of the above	[b]	

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- 20. Addition of pentavalent impurity to a semiconductor creates many .......
- a) Free electrons
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Department of Electronics and Communication Engineering

Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM Name of the Student: Godgepati Manjula ROLL Number: 2	D&BIAC	408
1. Which phenomenon is not reduced by the circuit paths of lowest impedances provided by power and return planes for shielding purposes?  a) Radiation		
b) Convection		
c) Noise		-
d) Crosstalk	[b]	V
2. Which among the below stated soldering methods is also renowned as 'High	Frequenc	y
Resistance Soldering'?		
a) Iron Soldering		
b) Furnace Soldering		
c) Torch Soldering	1	
d) Electrical Soldering	[d]	
3. Which among the below mentioned approaches belongs to the category of la	n-circuit	
Testing?		
a) Impedance Testing		
b) Component Testing		
c) Apply Signal and check output	4	./
d) All of the above	d	V
4. What is/are the necessity/ies to provide guarding to precision differential an	iplifiers?	
a) To increase leakage resistance		
b) To reduce capacitance between signal conductors & ground		
c) Both a and b		1/
d) None of the above	[0]	
5. When a pentavalent impurity is added to a pure semiconductor, it becomes		
a) An insulator		
b) An intrinsic semiconductor		
c) p-type semiconductor	. 1	
d) n-type semiconductor	[d]	
6. High current circuits are purposely located or placed near the edge of PCB	in	
accordance to the supply lines for		
a) Removal of heat		
b) Isolation of stray current		/
c) Reduction of path length	[0]	./
d) All of the above	[0]	V



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7. Which among the below mentioned packages does not belong to the category of	f 'Small
Outline Package'?	
a) SO	
b) SOP	
c) SOT	1 (
d) SON	[d] V
8. What effects can be observed if the separate power and ground planes are provi	ded
with large conducting surfaces for better decoupling in PCB layouts?	
a) Increase in self-inductance	
b) Reduction in self-inductance	
c) Stability in self-inductance	
d) None of the above	[a] V
9. Which among the below specified assertions is not a grounding consideration	
associated with ADC as well as DAC?	
a) Analog side to analog ground	
b) Digital side to digital ground	
c) Use of separate power supply and connection of their ground leads to single po	int
reference	1
d) Reduction of inductive loop area between power and return traces	[d] V
10. Which among the below stated devices/equipments are preferred for eliminati	
of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?	
a) Coupling capacitor	
b) Decoupling capacitor	
c) Snubber circuits	1 0
d) All of the above	[b]
11. Which among the below specified condition is precise in the crosstalk verification	ation
mechanism using logic flow in opposite direction with the limit of avoiding dange	
interference in digital PCB designing?	[C-]
a) $Z_{even} > Z_{odd}$	
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$	
c) $Z_{\text{odd}} \ge 0.8 Z_{\text{even}}$	
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12. Which terminology of PCB represents a thin photo-sensitive polymer by supp	orting
photographic pattern of single traces or IC pads for etching?	
a) Prepreg	
b) Etching	
c) Photo-resist	
d) Solder mask	[C] V
13. Which problems are about to occur if PCB is not designed properly in a confi	ned
manner for digital circuits?	
A. Diffraction	
B. Refraction	/
C. Ground & Supply-line Noise	1/
D. Electromagnetic Interference	[C]
a) A & B	
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b	) B & C		
C	) C & D		
C	) A, B, C, D		
1	4. Which type of solderability testing is carried out for the generation of solder sa	ample	
C	lue to immersion of wire or sheet metal specimen in a bath of molten solder?		
	) Solder Bath Testing		
t	Meniscus Rise Testing		
	Solder Iron Testing		1/
	None of the above	[b]	V
	5. Which among the following assists in obtaining the desired value of wave imp	edance	e
	n reflection phase while designing digital PCBs?		
	A. Width of signal lines		
	B. Distance between signal line and ground line		
	C. Signal Delays		
	D. Double Pulsing		
	a) A & B		
	o) B & C		
	c) C & D		,
	d) A, B, C, D	[0]	1
	16. What should be the resistance of 0.6 mm wide conductor with 15 cm length a	nd 25	V
	um thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6} (at 20^{\circ} C)$		
	a) $118.2 \text{ m}\Omega$		
	b) 138.2 mΩ		
	c) 172.4 mΩ		/
	d) 192.4 mΩ	[]	V
	17. The actual cost of PCB can be evaluated on the basis of		
	a) PCB size & material		
	b) Number of layers		
	c) Vias on PCB		1/
	d) All of the above	[d]	V
	18. Which factors contribute to the occurrence of mechanical stress?		
	a) Resonance		
	b) Cracked Solder Joints		
	c) Both a and b		
	d) None of the above	[b]	1
	19. Which type of PCB requires minimum soldering on component side in order	to avoi	id/
	replacement oriented difficulties?		
	a) Single-sided PCB		
	b) Double-sided PCB		
	c) Both a and b		1
	d) None of the above	[C]	X
			/ \



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- 20. Addition of pentavalent impurity to a semiconductor creates many .......
- a) Free electrons
- b) Holes
- c) Valence electrons
- d) Bound electrons

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## Certificate Program on PCB Design Assessment Marks

A.Y: 2021-2022

Year: II

S. No	Reg. No	Name of the Candidate	Marks
1	208B1A0401	ALLIBOYINA JHANSI LAKSHMI	19
2	208B1A0402	AMARTHALURI PRASANTHI	17
3	208B1A0403	BANDARU REETHIKA	18
4	208B1A0404	BANDARU SAI PRASANNA LAKSHMI	17
5	208B1A0405	CHODA AKHILA	18
6	208B1A0406	GOGULA NAGA MOUNIKA	19
7	208B1A0407	GONUGUNTLA THANMAI	18
8	208B1A0408	GORREPATI MANJULA	18
9	208B1A0409	GUNDLATHOTI ANJALI	18
10	208B1A0410	ILA THIRUPATHAMMA	19
11	208B1A0411	KASIREDDY UMA	18
12	208B1A0412	KONISAM TIRUPATHAMMA	19
13	208B1A0413	MAKKENA NAVEENA	19
14	208B1A0414	MARAM MALATHI	20
15	208B1A0415	MITHUKULLA AMULYA	16
16	208B1A0416	PULICHERLA ADILAKSHMI	19
17	208B1A0417	SHAIK KARISHMA	18
18	208B1A0419	SWARNA GAYATHRI	19
19	208B1A0420	TENALI SAI SUPRAJA	17
20	208B1A0421	TUMMAPUDI VENKATA LAKSHMI AKHILA	19
21	208B1A0422	UTUKURI LAKSHMIPRASANNA	16
22	208B1A0423	VALIVETI THANUJA	18
23	208B1A0424	VALLEPU ANUSHA	18
24	208B1A0425	YANNAM NAGA MALLESWARI	18
25	208B1A0426	YELCHURI LAKSHMI PRIYA	15
26	208B1A0427	ASUPALLI SIVA REDDY	19
27	208B1A0428	BOGISETTY SURYA PRAKASH	18
28	208B1A0430	GATTUPALLI VENKATA SAI KRISHNA SATHVIK	19
29	208B1A0431	GOGULA SUNIL SANDESH	17
30	208B1A0433	GUDIPATI VENKATA RAKESH	19
31	208B1A0434	MANCHALA VENKATESWARLU	16
32	208B1A0435	MARAMREDDY VISHNU VARDHAN REDDY	16
33	208B1A0436	MUNNANGI ADARSH	16
34	208B1A0437	MYPATI ASHOK KUMAR	17

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S. No	Reg. No	Name of the Candidate	Marks
35	208B1A0438	PALLABOTHULA PRASANTH	18
36	208B1A0439	PATHAKAMURI LOKESH	16
37	208B1A0440	POTTURI VENKAT KARTHIKEYA	19
38	208B1A0441	PULLELA VENKATA SAI KUMAR	18
39	208B1A0442	PURANAM MANIKANTA	19
40	208B1A0443	SAPPARAPU SYAM	18
41	208B1A0444	SHAIK TIPPU FIROZ	17
42	208B1A0445	SINGAMSETTY VENKATA SAI SUBHASH	18
43	208B1A0446	SINGARAJU ARAVIND	17
44	208B1A0447	SYED JILANI	18
45	208B1A0448	VARIKUTI ANIL REDDY	19
46	208B1A0449	VEMULA BALAKRISHNA	18
47	208B1A0450	YALLAVULA MANOHAR REDDY	18
48	208B1A0451	AMARA LAKSHMI MOUNIKA	17
49	208B1A0452	BHAVANAM KEERTHI	19
50	208B1A0453	BHUPATHI ANUSHA	20
51	208B1A0454	BISAI SIREESHA	20
52	208B1A0455	BOLLA MAMATHA	16
53	208B1A0456	BUSI JYOSHNA	19
54	208B1A0458	DESAM NAGAMANI	16
55	208B1A0459	DEVARAPALLI HARSHITHA	20
56	208B1A0460	IDAMAKANTI SRAVANI	16
57	208B1A0461	KASIREDDY VASUNDHARA	19
58	208B1A0462	KOLIKI SIRISHA	18
59	208B1A0463	MUPPARAJU SRAVANI	19
60	208B1A0464	PALAGUMMI GNANA VENKATA RAJANI	18
61	208B1A0465	PALLAPU AMANI	17
62	208B1A0466	PERISOMULA VASAVI HANVITHA	17
63	208B1A0467	POTHURAJU LAKSHMI PRATHYUSHA	17
64	208B1A0468	VALLEPU NAGASIVA	19
65	208B1A0469	ALUGUNDLA VENKATA SIVA REDDY	16
66	208B1A0470	AMARTHALURI NAGA VAMSI	19
67	208B1A0471	AMBATI MANOHAR SAI	19
68	208B1A0472	BADITHALA SAI VAMSI KRISHNA	20
69	208B1A0473	BASAM HEMANTH KUMAR	17
70	208B1A0474	BHIMISETTY SUDHEER BABU	18
71	208B1A0475	CHIMMIRI BALAJI	18

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#### Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
72	208B1A0476	CHINTAM KUMAR	19
73	208B1A0477	CHUNDURI VAMSI	19
74	208B1A0478	DASARI VENKATA RISHI RAMANAND	19
75	208B1A0479	G S RANJITH KUMAR REDDY	20
76	208B1A0480	GUNDEBOMMA SIVA SANKAR PRASAD	20
77	208B1A0481	GUNIMINI SAI KIRAN	20
78	208B1A0482	KATTA VASU	19
79	208B1A0483	KONGARA KARTHIK	18
80	208B1A0484	KONKA NARENDRA	17
81	208B1A0485	KUNCHALA SRIKANTH	18
82	208B1A0486	KUNCHALA TARUN	17
83	208B1A0487	KUNCHELA SRI HARI	18
84	208B1A0488	MADALA VENKATESWARLU	19
85	208B1A0489	METTA PAVANKALYAN	18
86	208B1A0491	PATAN SURAJ KHAN	18
87	208B1A0492	POKA MAHESH BABU	17
88	208B1A0493	PUSALA RAMAN TARUN TEJA	19
89	208B1A0494	PUTTA VENKATA THARUN KUMAR	20
90	208B1A0495	SRUNGARAPU VENKATA SAI AKASH	20
91	208B1A0496	SUNKARI NARASIMHA NAIDU	20
92	208B1A0497	TANIKONDA GANESH	20
93	208B1A0498	THAPPETA SAMPATH KUMAR	20
94	208B1A0499	THULASI DINESH KUMAR	17
95	208B1A04A0	UDAYAGIRI HARSHITH	19
96	208B1A04A1	UPPU DINESH	18
97	208B1A04A2	YADALA MANI KANTA	19
98	208B1A04A3	YENUBARI PRAMOD SAGAR	19
99	208B1A04A4	NAGINENI RAMUDU	19
100	218B5A0401	GOURAVARAPU HARISHA	19
101	218B5A0402	NALAMOTHU KALYANI	19
102	218B5A0403	PURINI SINDHUJA	19
103	218B5A0404	PYDALA PRANAVI	19
104	218B5A0405	SODA DIVYA	19
105	218B5A0406	TIPPABATHINA PRASANNA LAKSHMI	18
106	218B5A0407	VARIKALLU PREMANKITHA	18
107	218B5A0408	YEDLURI NEERAJA	19





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Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
108	218B5A0409	BADAM ASHOK REDDY	18
109	218B5A0410	DAADI YASWANTH SRINIVAS	16
110	218B5A0411	ETIPOGU DEVID	19
111	218B5A0412	GUMMOJI VENKATA LOKNATH	19
112	218B5A0413	KAMJULA YASHWANTH RAGHAVA REDDY	20
113	218B5A0414	PAPPU BHANU PRAKASH	18

Coordinator

HEAD OF THE DEPARTMENT Department of E.C.E. RISE Krishna Sai Gandhi Group

of Institutions VALLURU, A.P.-523 272

PRINCIPAL
RISE KRISHNA SAI GANDHI
GROUP OF INSTITUTIONS
VALLURUS ONGOLE.

## RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS: ONGOLE DEPARTMENT OF ECE

Certificate program on PCB Design 21-02-2022 to 25-02-2022

The Certificate Program conducted by ECE department on 21th - 25th Feb - 2022 in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS in association with Center for Electronics System Design (CESD)

Department of Electronics & Communication Engineering



RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

## Objectives of conducting Certificate program

- To make students learn and interact with renowned industry experts.
- Make Students to receive an unparallel education on the art of PCB Designing Certificate program with personal one on one attention.
- To make every student an expert in designing their own **PCB board** which would be very useful for developing their own projects.

#### Overview about Certificate Program:

The aim of this **Certificate Program** is to make the students learn the designing and manufacturing of a printed circuit board using open source KICAD PCB design software and with various active and passive components such as Regulators, Diodes, Resistors, Capacitors, Inductors, Switches, e.t.c.

#### **Technical Support:**

The Certificate Program was conducted in collaboration with Center for Electronics System Design (CESD) from Vijayawada. The company has a fast growth in PCB designing. The company's director Mr. Finney Daniel accompanied with Seven Trainers attended the Certificate Program for guiding the students in learning the technologies of the PCB Design Certificate Program. They have taken about 32 hours of theoretical and practical sessions.

#### Department of ECE:

Department of ECE has taken the opportunity to conduct the in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS. As the theme of the Certificate Program is the core for the department, it's a nice opportunity for the students to learn the technology and to implement that practically.

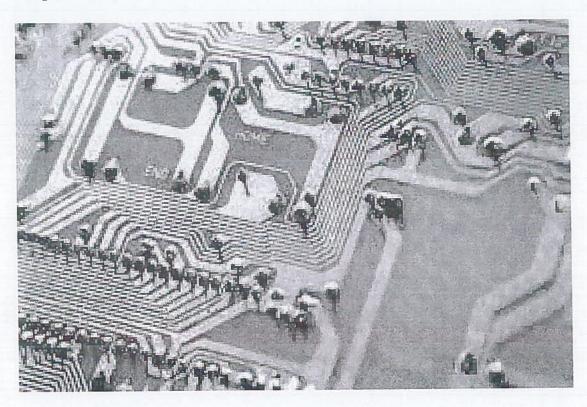
#### Technical Report on Certificate Program:

The Technical team of Center for Electronics System Design (CESD) has described the entire designing process in a step by step procedure.

#### 1. Basic PCB Concepts

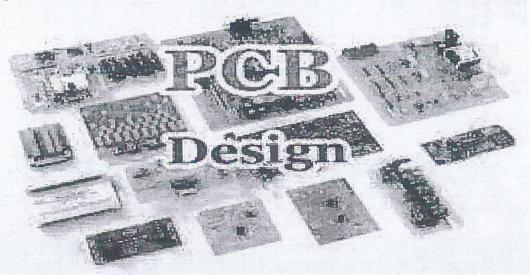
First of all they have given the concepts which will be very helpful for designing the PCB practically, using some power point presentations. In this theoretical explanation part they have explained about the KI-CAD software and the use of software for further practical implementation in designing the PCB. They have also

RISE KRISHNA SAI GANDHA GROUP OF INSTITUTIONS VALLURU: ONGOLE. given a briefing about active and passive electronic components which they will be using in a PCB.



## 2. Editing and Routing

Editing and Routing is the basic step and it is one of the important step for designing a PCB. Editing and Routing gives the circuit layout from one component to the other components. Soldering plays a key role in this step.



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### 3. Creation of Library and Components & Report Generation

This is a step done using KI-CAD tools. In this step the components in the circuit and the respective libraries are selected in this software. So that the required circuit will be designed in the software and a print of the same will be taken on a sheet. The same print will be useful for the further process.

#### 4. Toner Transfer Method

This is the step where the designed circuit will be pasted on the wafer and this will be passed through a temperature of about 160 to 180 degrees so that the tracks of the circuit will be remained on the wafer. The tracks will be a conductive type.

#### 5. Drilling Technique

The board will be drilled with holes where the components have to be placed; the holes will be drilled in the board depending on the terminals available for the components in the design. The hole should be in the size so that the terminal has to be freely placed in the hole.

#### 6. Soldering Technique

The components that are placed in the board should be soldered to the track so that the circuit is connected as per the design. After this step the engraved PCB will be ready to use.

The Department conducted test on PCB Design for Electronic components and all project models are exhibited in the respected department

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## Student Response

Almost 113 students had taken part in the Certificate Program. All the students responded that they have learned and had hands on experience in designing a PCB. They are very excited in participation in this Certificate Programand requested for more Certificate Program in similar way so that they can simultaneously gain the practical knowledge.

## Distribution of Certificates

At the last day question answer session and certificate distribution function started on 4:30 PM. Feedbacks regarding workshop are provided by various students.

All the students were awarded with a participation certificate from the company Center for Electronics System Design (CESD). Principal Dr.K.V.Subrahmanyam garu awarded the certificates to all the students by hand. He personally congratulated every student for participating in the event and making it successful.

RISE KRISHMA SANGANDIN

VALLURUS DAGS E

#### Vote of Thanks

Mr.S V Ravi Kumar beloved HOD of ECE Department thanked every student for their active participation and interest in participating in the Certificate Program and mentioned about the activities conducted in the college by the department. He promised that department will continue its assistance in conducting these sorts of Certificate Programs and seminars in future.

He thanked the technical support given by Center for Electronics System Design (CESD). He personally felt very happy for the response of the company and satisfied with the way they conducted the Certificate Program.

He mentioned about the marvelous support given by the Principal Dr.K.V.Subrahmanyam garu to the department in conducting these Certificate Program. He also thanked for the personal interest taken by him in encouraging the department in all aspects.

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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

Date: 25-02-2022.

### **CLOSING REPORT**

To, The Principal, RISE Krishna Sai Gandhi Group of Institutions.

As per the approved schedule, the ECE department has conducted a Certificate Program on "PCB Design" at ECE Seminar hall from 21-02-2022 to 25-02-2022. 113 students of II ECE have participated in this program. Sri **F.Daniel**, Director, Center for Electronics Systems Design (CESD), Vijayawada, AP, acted as the resource person for this program.

Main issues addressed:

- 1. Basic PCB Concepts
- 2. Editing and Routing
- 3. Creation of Library and Components & Report Generation
- 4. Toner Transfer Method
- 5. Drilling Technique
- 6. Soldering Technique

We are expecting your support in future also. Thanking you sir,

Coordinator

(200860)

PRINCIPAL
RISE KRISHNA SAI GANDHI
GROUP OF INSTRUCTIONS
VALLURU: COLUMN

Yours faithfully,

HOD HOD

Department of E.C.E.
RISE Krishna Sai Gandhi Group
of Mittutions, VALLURU, A.P.-523 277