Department of Electronics and Communication Engineering



On

"PCB Design"

Date: 14<sup>th</sup>to 18<sup>th</sup> NOV - 2022

## Finney Daniel

Dirctor,center for electronics system design Vijayawada

> PRINCIPAL DISHMA PALCAN

GROUP OF INSTITUTIONS



(Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada) NH-16, Valluru, Ongole, Prakasam (District)-523272

Valluru,

Date: 03-10-2022

To

F.Daniel, Dirctor, Center for Electronics System Design, Vijayawada.

Dear Sir,

Subject: Inviting for Certificate program - Reg.

Greetings from RISE Krishna Sai Gandhi Group of Institutions, Ongole

As per the discussion with Dr.K.V.Subrahmanyam, Principal, of our Institute, I hereby take this opportunity to invite you to conduct the Certificate program on **PCB Design** "From 14-11-2022 to 18-11-2022.

You are requested to interact and provide guidance to our II B.Tech students, who are looking forward to their bright career ahead. I will feel honored by your gracious presence at our organization. I believe that your lecture will help our students and faculty members to explore knowledge.

Thanking you in anticipation.

Yours sincerely,

PRINCIPAL

RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

VALLURU:: ONGOLE.

PISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS

VALLURU:: ONGOLE.

## **Finney Daniel**

Managing Director
Center for Electronics System Design

#### **Personal Summary**

Finney Daniel has a record of organizing Institutional Industry oriented up-gradation programs for undergraduates. Experienced in delivering recent trend technologies to the personnel in vivid methodologies. Providing a lawn of possibilities in the specified area which strengthen the personnel in growing the skills required for their success in the present day competence. He has experience as a guest lecturer, assistant professor and a research fellow. His main interest in this has been to prove the potential and ability of the personnel.

#### **Professional Summary**

- Delivered services as Guest Lecturer for VLSI in Andhra University College of Engineering.
- Worked as Assistant Professor in couple of Engineering Colleges.
- As Junior Research Fellow in Defence Research & Development Laboratory.

#### Areas of Expertise

- **Product Development:** Evolving modules that enable a final product meeting the End- User requirements and facilitate easy utility of the product
- Project Management: Maintaining strategic planning and supporting the team in delivering Robust Models by providing employ friendly platform.
- Organizing Training Sessions: Planned tabulation for training and hands on expertise for the personnel under training.

#### **Professional Skills and Competencies**

- Strong knowledge on Software tools like QUARTUS, Xilinx, Cadence, Tanner- EDA, Mentor-Graphics required for VLSI.
- Good knowledge on hardware design and development includes familiarity in Embedded System tools and PCB design tools like MPLAB Xpress IDE, KEIL, Micro-c, ZUKEN- Cadstar, Eagle, Express-PCB.

PRINCIPAL

RISE KRISHIVA SAI GANDHI

CROUP OF INSTITUTIONS

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#### **Key Roles**

- Academic Director for KR's Educational Society.
- Coordinator for Technical Symposium in Holy Mary Group of Institutions.
- Organized Workshops on Verilog, PCB Design, Prototyping, Embedded Systems, Product Design and Development.

#### Qualification

- Master of Technology in VLSI-System Design from JNTU-Kakinda.
- PG Diploma in Electronic Product Design from Electronics System Design and Manufacturing (ESDM, Govt. of India).
- Graduation in Electronics & Communication Engineering from CJITS, JNTU- Hyderabad.
- Graduation in Bachelor of Science in Mathematics from Andhra University.

#### **Personal Details**

- Born on 21<sup>st</sup> June 1987 in Visakhapatnam.
- Indian citizen and can speak Hindi, English, Telugu.

References - Available on Request.

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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

#### PROPOSAL FORM

SUB: Certificate program - Program.

## TO THE SECRETARY/CORRESPONDENT THROUGH PRINCIPAL FOR KIND APPROVAL

1	NAME OF THE INSTITUTION	Rise Krishna Sai Gandhi Group of Institutions
2	NAME OF THE DEPARTMENT	Electronics & Communication Engineering
3	TITLE OF THE PROGRAMME	Certificate program
4	NAME OF THE PROGRAMME	Certificate program on "PCB Design for Electronic Designs"
5	OBJECTIVE OF THE PROGRAMME	To bring the exposure in the PCB Design.
6	DETAILS OF RESOURCE PERSON(S)& CV ATTACHED.	Finney Daniel Director, center for electronics system design Vijayawada.
7	PROPOSED DATE(S)/ACADEMIC YEAR	14-11-2022 to 18-11-2022
8	DURATION OF THE PROGRAMME	FIVE DAY
9	VENUE	Seminar Hall
10	TARGETS	II ECE students
11	No. OF PARTICIPANTS	132 Students
12	REGISTRATION FEE	Free
13	NAME OF PROGRAMME CO ORDINATOR(S)	Mr. K.Nagahanuma Chari
14	NAME OF THE STUDENTS COORDINATOR(S)	1.Ms. Pilli Ammulu (218B1A0424) 2.Mr. Velugolu Vikas (228B5A0406)





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Department of Electronics and Communication Engineering

15	SOURCE OF FUND IDENTIFIED	Management
16	MANAGEMENT CONTRIBUTION REQUIRED	YES
17	PROPOSAL PREPARED BY	Mr.K.Nagahanuma Chari (CO-ORDINATOR)

S. V ODAOD & ? HEAD OF THE DEPARTMENT
Department of E.C.E. RISE Krishna Sai Gandhi Group of Institutions, VALLURU, A.P.-523 272

KRISHNA SAI GANDHI GROUP OF INSTITUTIONS VALLURU: ONGOLE.



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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

Valluru, Date: 11-11-2022.

#### CIRCULAR

This is to inform II B.Tech students and faculty that there will be a 5-Day Certificate program on "PCB Design" from 14-11-2022 to 18-11-2022 by F.Daniel, Director, Center for Electronics System Design, Vijayawada.

Copy to:

Principal

Staff Circular

Students of ECE II year

ECE Department Notice Boards

CAD OF THE DEPARTMENT

RISE Krishna Sai Gandhi Group

of Institutions, VALLURU, A.P. 523 272

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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

#### Certificate Program on "PCB Design"

Date: 14<sup>th</sup>to 18<sup>th</sup>November 2022

#### SCHEDULE FROM 14-11-2022 TO 18-11-2022

S. No	Program List	Timing			
		From	То		
Eal	DAY - 01 (14-11-20	)22)			
1	Program started	09.00 AM			
2	Lamp lighting	09.00 AM	09.10 AM		
3	Principal speech	09.10 AM	09.25 AM		
4	HOD Introduction about PCB Design	09.25 AM	09.35 AM		
5	Tea Break	09.35 AM	10.00 AM		
6	Introduction about PCB concepts	10.00 AM	01.00 PM		
7	Lunch Break	01.00 PM	01.45 PM		
8	KI-CAD Software Practical Section	01.45 PM	05.00 PM		
	DAY - 02 (15-11-2	022)			
9	Concepts of PCB Designing, PCB Materials, Layers	09.00 AM	12.15 PM		
10	Lunch Break	12.15 PM	01.00 PM		
11	Multilayer Concepts	01.00 PM	05.00 PM		
**	DAY - 03 (16-11-2	022)			
12	PADSTACK	09.00 AM	12.15 PM		
13	Lunch Break	12.15 PM	01.00 PM		
14	Schematic entry KI-CAD tools	01.00 PM	05.00 PM		
	DAY - 04 (17-11-2	022)			
15	Drawing a schematic FLAT	09.00 AM	12.15 PM		
16	Lunch Break	12.15 PM	01.00 PM		
17	BOM. Net list generation	01.00 PM	05.00 PM		
	DAY - 05 (18-11-2	022)			
18	Designing Boards	09.00 AM	12.15 PM		
19	Lunch Break	12.15 PM	01.00 PM		
20	Drawing a schematic HIERARCHICAL Design	01.00 PM	04.15 PM		
21	Certificate Program Exam	04.15 PM	04.45 PM		
22	Vote of Thanks	04.45 PM	05.00 PM		

Coordinator

PRINCIPAL

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#### RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMET OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Student: N. VYShrowi
Roll No Roll No : 218B1A0421
Topic : Certificate Program on "PCB Design"

Date: 18-11-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?	1				
2	Is the certification program well planned or not?	1				
3	Lecture makes objectives clear?	$\checkmark$				
4	Lecture speaks clearly and audibly?		~			
5	Lecture explains with exaples clearly?	· ~				
6	Is you are doubts clarified or not?	/				

5-Excellent 4-Good 3-Average 2-Poor 1- No comment

> Note. Student Signature

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#### RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

#### Student Feedback Form

Name of the Student: Tamolya

Roll No : 20810100430 Topic : Certificate Program on "PCB Design"

Date: 18-11-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?	~				
2	Is the certification program well planned or not	? 🗸				
3	Lecture makes objectives clear?					
4	Lecture speaks clearly and audibly?					
5	Lecture explains with exaples clearly?	/				
6	Is you are doubts clarified or not?					
5-Exc	ellent 4-Good	3-Average	2-Poor	Valleton Valleton	1-Noc	omment

T. Amulya Student Signature



## RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

#### Student Feedback Form

Name of the Student: PANOL DOCATE

Roll No : 21861A0456
Topic: Certificate Program on "PCB Design"

Date: 18-11-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?		~			
2	Is the certification program well planned or not?		~			
3	Lecture makes objectives clear?					
4	Lecture speaks clearly and audibly?	1				
5	Lecture explains with exaples clearly?		~			
6	Is you are doubts clarified or not?	~				

5-Excellent

4-Good

3-Average 2-Poor

1- No comment

P.Noveen Student Signature

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VALLURU: ONG



#### RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

#### **Student Feedback Form**

Name of the Student: B. Aphila

Roll No : 2(8B(10040) Topic : Certificate Program on "PCB Design"

Date: 18-11-2022

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?	~				
2	Is the certification program well planned or not?		~			
3	Lecture makes objectives clear?		/	·		
4	Lecture speaks clearly and audibly?		/			
5	Lecture explains with exaples clearly?		~			
6	Is you are doubts clarified or not?	~				

5-Excellent 4-Good 3-Average 2-Poor

1- No comment

Student Signature



# RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING CERTIFICATE PROGRAM FEEDBACK ANALYSIS

A.Y: 2022-2023

Year: II B. Tech ECE

Date: 18-11-2022

S.No	Roll Number	Name	1	2	3	4	5	6
1	218B1A0401	BANDARU AKHILA	5	4	.4	4	4	5
2	218B1A0402	BODEY SEETHA MAHALAKSHMI	5	5	5	5	5	5
3	218B1A0403	BOMMISETTY NAGA NIKITHA	4	5	4	5	4	4
4	218B1A0404	CHAPPIDI SUPRITHA	5	4	4	4	5	5
5	218B1A0405	VALLAMSETTI VENKATA NAGA ANUSHA	5	5	5	5	5	5
6	218B1A0406	DARSI SWATHI	5	5	5	5	5	5
7	218B1A0407	DHUPATI KAVITHA	5	5	5	5	5	5
8	218B1A0408	DIVVELA PUJITHA	5	5	5	5	5	5
9	218B1A0409	DUPATI APARNA	5	5	5	5	5	5
10	218B1A0410	GIDDA ANJALI	5	4	5	4	5	5
11	218B1A0411	GOGINENI DEEPTHI	5	5	5	4	5	.5
12	218B1A0412	GOSU JAYA SRI	5	5	5	5	5	5
13	218B1A0413	KARIDHU KALYANI	5	4	5	5	5	5
14	218B1A0415	KOKKILIGADDA BHAVANI	4	5	5	5	5	5
15	218B1A0416	KONIKI POOJITHA	.5	5	4	5	5	5
16	218B1A0417	KONIKI PRAVALLIKA	5	5	4	5	4	5
17	218B1A0418	MANNEM DEEPIKA JYOTHI	5	5	5	4	5	4

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S.No	Roll Number	Name	1	2	3	4	5	6
18	218B1A0419	MURAKONDA VENKATA JASMITHA	5	4	4	5	4	5
19	218B1A0420	NARIPEDDI VENKATASIVANAGARAJA	5	5	5	4	4	5
20	218B1A0421	NELAPATI VYSHNAVI	5	5	5	4	5	5
21	218B1A0422	PABOLU APARNA	5	4	5	5	4	5
22	218B1A0423	PAVANI ANUPRAVALLIKA	5	5	5	4	5	5
23	218B1A0424	PILLI AMMULU	5	5	4	4	5	5
24	218B1A0425	POKURI NANDINI	5	5	4	5	5	5
25	218B1A0426	REVURI VIJITHA	5	5	4	5	5	5
26	218B1A0427	SHAIK KARISHMA	5	5	5	4	4	5
27	218B1A0428	SHAIK SHIRAJ UNNISA BEGUM	4	5	4	5	5	5
28	218B1A0429	SYED NOORI	5	5	4	5	5	4
29	218B1A0430	TENALI AMULYA	5	5	5	5	5	5
30	218B1A0432	AKULA MOHAN VAMSI NADH	5	5	4	5	4	. 4
31	218B1A0433	ALAHARI RAMESH	4	5	4	5	5	5
32	218B1A0434	DAMA MANIKNTA	5	5	5	5	4	5
33	218B1A0435	ANUMALA PRAVEEN	4	5	4	5	5	5
34	218B1A0436	ARIBOYINA DHARMA TEJA	5	5	4	4	5	5
35	218B1A0437	BOGISETTY PREMCHAND	5	5	4	4	5	4
36	218B1A0438	BOTTU YASWANTH	5	5	4	5	4	4
37	218B1A0439	CHAVATAPALEM SIVA SANKAR	4	4	4	5	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
38	218B1A0440	CHILAKAPATI SHANMUKHA SAI RAM	5	4	4	4	5	4
39	218B1A0441	CHINNAPUREDDY KOTIREDDY	4	5	4	5	5	4
40	218B1A0442	DEVARAPALLI HARSHAVARDHAN	5	4	5	5	5	4
41	218B1A0443	ENUGU HARSHA VARDHAN	5	5	4	5	4	4
42	218B1A0444	GADDALA ISSAKU	5	4	4	4	5	4
43	218B1A0445	GUNJI ACHYUTH	4	5	4	5	5	4
44	218B1A0446	KALAPALA SIVARAMABRAHMACHARI	5	5	5	4	4	4
45	218B1A0447	KANTA GOVINDAIAH	4	5	4	5	5	5
46	218B1A0448	KATTA SASI KUMAR	4	4	4	5	5	4
47	218B1A0449	KOKKILAGADDA ASHOK KRISHNA	5	4	4	5	5	4
48	218B1A0450	KOTA DINESH	4	5	5	4	4	4
49	218B1A0451	MEDAM HARSHITH	4	5	5	5	5	5
50	218B1A0452	LAKKAMRAJU ADI SANKARA NARAYANA RAJU	4	4	5	4	4	4
51	218B1A0453	LAKKIREDDY VEERA VENKATA PRATHAP REDDY	5	4	5	5	5	4
52	218B1A0454	MULE VENKATESWARLU	5	4	5	5	5	4
53	218B1A0456	PASAM NAVEEN	4	4	4	5	4	5
54	218B1A0457	PATAN SALLAUDDIN	5	5	5	4	5	5
55	218B1A0458	PILLI BRAHMA REDDY	4	5	5	5	5	5
56	218B1A0459	PUTTA NAVINESH REDDY	5	5	5	4	5	5
57	218B1A0460	PUVVADA YASHWANTH KUMAR	4	5	5	4	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
58	218B1A0461	SHAIK JANIBASHA	5	4	5	5	4	4
59	218B1A0462	SHAIK MUNEER AHAMAD	4	5	5	4	5	5
60	218B1A0463	SHAIK SAMEER	5	4	5	5	5	5
61	218B1A0464	SWARNA GOPI	4	5	5	4	5	5
62	218B1A0465	TANGUTURI PAVAN KUMAR	5	5	5	4	5	5
63	218B1A0466	UPPALAPATI SRINU	5	5	4	4	5	5
64	218B1A0467	ELAPALAPATI NAVYA TEJA	5	5	5	5	5	5
65	218B1A0468	ALAHARI SRI PRIYANKA	4	5	5	4	5	5
66	218B1A0469	BANDELA SANJAMMA	5	5	5	4	5	5
67	218B1A0470	BAPIREDDY SNEHA LATHA	4	4	5	4	5	5
68	218B1A0471	BOLLAVARAM SHREYA	5	5	5	5	4	4
69	218B1A0472	DASARI NANDINI	5	5	5	5	5	5
70	218B1A0474	GADDALA SUBHASHINI	5	4	4	5	5	5
71	218B1A0475	INDLA GIRIJA	4	5	5	5	4	5
72	218B1A0476	JASTI SIREESHA	5	5	5	5	5	5
73	218B1A0477	KAMASANI ANUSHA	5	5	4	4	5	5
74	218B1A0478	KODURI SIRISHA	5	5	5	5	5	-5
75	218B1A0479	KONDURI PUJITHA REDDY	5	4	5	5	4	4
76	218B1A0480	KOTTURI GAYATHRI	4	5	5	5	5	5
77	218B1A0481	KUKATLA AMULYA	5	5	5	5	4	5

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S.No	Roll Number	Name	1	2	3	4	5	6
78	218B1A0482	KUMMITHA AMULYA	5	4	4	5	5	4
79	218B1A0484	MALIREDDY CHANDU PRIYA	4	5	5	5	5	5
80	218B1A0485	MEDIKONDA MANISHA	5	5	5	5	4	5
81	218B1A0486	MIDASALA PRAVALLIKA	5	. 5	4	5	5	5
82	218B1A0487	NALAGANGA PRAVALLIKA	5	5	5	5	4	5
83	218B1A0488	NALLABOTHULA SULOCHANA	4	5	5	4	4	4
84	218B1A0489	NALLURI KAVYA	5	5	5	4	4	5
85	218B1A0490	ORCHU DURGA	4	5	5	5	5 ,	5
86	218B1A0491	PATAN ISHRATH	5	5	4	5	4	4
87	218B1A0492	PERAM VENKATA SAI VANI	5	5	5	5	5	5
88	218B1A0493	POKURU LAKSHMI SOWJANYA	4	5	4	5	5	5
89	218B1A0494	RASIM LAKSHMI BHAVANI	5	5	5	4	5	5
90	218B1A0495	REDITHI AKSHAYA	5	4	5	5	5	5
91	218B1A0496	SANNEBOINA THULASI	5	4	4	5	5	4
92	218B1A0497	SANNEBOYINA SRI LAKSHMI	4	5	5	4	5	5
93	218B1A0498	SOMINENI AMULYA	4	4	5	5	4	4
94	218B1A0499	SURA ANUSHA	5	5	4	5	4	5
95	218B1A04A0	SURAM NANDINI	4	4	5	5	5	5
96	218B1A04A1	UDAYAGIRI CHENCHAMMA	4	4	5	5	4	4
97	218B1A04A2	UTUKURI KALYANI	- 5	> 4	4	4	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
98	218B1A04A3	VELUGOLU VENKATA ANANTHA LAKSHMI	4	4	5	5	4	5
99	218B1A04A4	YARAM ANKITHA	4	5	5	4	5	4
100	218B1A04A5	YENIMIREDDY VINEELA	4	4	4	5	5	5
101	218B1A04A6	ATHANTY ARUN KUMAR	4	5	5	Ŝ	5	5
102	218B1A04A7	AVVARU VENKATA GANESH	4	4	5	4	5	4
103	218B1A04A8	BATHINA AKHIL	4	5	5	5	5	5
104	218B1A04A9	DANDEBOYINA MAHESH	4	4	5	5	5	5
105	218B1A04B0	DHARNASI RAKESH	5	5	4	4	5	4
106	218B1A04B1	GUDLURU BHANUPRAKASH	4	5	5	4	5	5
107	218B1A04B2	KAKARLA MANOHAR	4	5	4	5	5	5
108	218B1A04B3	KAKUNURI VENKATA DURGA PRASAD REDDY	4	4	5	5	5	5
109	218B1A04B4	KALLURI DINESH BABU	5	5	5	5	5	5
110	218B1A04B5	KASU RADHAKRISHNA	4	5	4	5	5	4
111	218B1A04B6	KAVURI BALA VIGNA MANI KANTA	4	4	5	4	5	5
112	218B1A04B7	KONIKI SHIVAJI	4	4	5	4	4	4
113	218B1A04B8	KURRA BALARAJU	5	4	4	4	4	5
114	218B1A04B9	ERISETTY SRINIVASULU	5	5	5	5	5	5
115	218B1A04C0	MASUNURI VENKATA KASI NAGA MANIKANTA	5	4	5	4	4	4
116	218B1A04C1	MEDAM VENKATA VISHNU VARDHAN REDDY	5	4	5	5	5	5
117	218B1A04C2	PODILI VEERA HANUMA	(i)	5	4	4	4	5

PRINCIPAL
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S.No	Roll Number	Name	1	2	3	4	5	6
118	218B1A04C3	SHAIK AYAAZ	4	4	5	4	5	4
119	218B1A04C4	THATIKONDA VENKATA VAMSI	5	4	5	4	5	5
120	218B1A04C5	THOKA KARUNAKAR	5	4	5	4	5	5
121	218B1A04C6	YADLA MADESH REDDY	5	5	4	4	4	5
122	228B5A0401	AYINAMPUDI GIREESH KUMAR	5	5	4	5	4	4
123	228B5A0402	CHEREDDY SUBRAHMANYAM	5	4	4	4	5	5
124	228B5A0403	MANGOLLU NIKHILA	5	5	4	5	5	5
125	228B5A0404	RAVULAPALLI AMARNADH	5	4	5	4	4	5
126	228B5A0405	SINGAMREDDY MALYADRI	5	5	5	4	4	4
127	228B5A0406	VELUGOLU VIKAS	5	4	5	4	4	4
128	228B5A0407	APPADI RAJ KUMAR	4	5	5	4	4	4
129	228B5A0408	GOLLAPOTHU YASWANTH	5	4	5	4	5	4
130	228B5A0409	RAYANA PAVAN KUMAR	5	4	4	5	5-	5
131	228B5A0410	TANNIRU HARSHA VARDHAN	5	4	5	5	5	5
132	228B5A0411	KOPPARTHI AKHIL	5	5	5	5	5	5
	Terral E-File		4.57	4.45	4.66	4.41	4.66	4.66
			91.43	88.97	93.10	88.28	93.10	93.10

Coordinator

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Department of E.C.E.
RISE Krishna Sai Gandhi Group.
of Institutions, VALLURU, A.P.-523 272



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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

#### Certificate program Feedback Analysis

Topic : Certification program on" PCB Design"

Resource Person : F.Daniel

Director, center for Electronics System Design, Vijayawada

Dates : 14-11-2022 to 18-11-2022

Venue : Seminar Hall

Targeted Students : II Year students

S.No	No. of students Participated	No. of students given feedback	Feedback %
1	132	132	100%

Coordinator

S.V. don' &

HEAD OF THE DEPARTMENT Department of E.C.E. RISE Krishna Sai Gandhi Group of institutions, VALLURU, A.P.-523 272

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Department of Electronics and Communication Engineering

#### Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM	
Name of the Student:	ROLL Number:
1. Which phenomenon is not reduced by the circuprovided by power and return planes for shielding	uit paths of lowest impedances especially ng purposes?
a) Radiation	
b) Convection	
c) Noise	[]
d) Crosstalk	Lada is also renovemed as 'High Frequency
2. Which among the below stated soldering met	hous is also renowned as Tright Frequency
Resistance Soldering'?	
a) Iron Soldering	
b) Furnace Soldering	
c) Torch Soldering	
<ul><li>d) Electrical Soldering</li><li>3. Which among the below mentioned approach</li></ul>	2 2
	ics belongs to the eategory of in entert
Testing?	
a) Impedance Testing b) Component Testing	
c) Apply Signal and check output	
d) All of the above	
4. What is/are the necessity/ies to provide guard	ling to precision differential amplifiers?
a) To increase leakage resistance	
b) To reduce capacitance between signal condu	ctors & ground
c) Both a and b	
d) None of the above	
5. Which among the below mentioned assertion	is is not a way of cross-talk reduction
while designing digital PCBs?	
a) Decrease in the distance between conductors	
b) Shielding of clock lines with guard strips	
c) Reduction in the loop area of circuits	
d) Avoid running of parallel traces for longer d	istances especially for asynchronous
signals	
6. High current circuits are purposely located of	or placed near the edge of PCB in
accordance to the supply lines for	
a) Removal of heat	
b) Isolation of stray current	
c) Reduction of path length	
d) All of the above	

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#### Department of Electronics and Communication Engineering

7. Which among the below mentioned packages does not belong to the category of 'Smal
Outline Package'?
a) SO
b) SOP
c) SOT
d) SON
8. What effects can be observed if the separate power and ground planes are provided
with large conducting surfaces for better decoupling in PCB layouts?
a) Increase in self-inductance
b) Reduction in self-inductance
c) Stability in self-inductance
d) None of the above
9. Which among the below specified assertions is not a grounding consideration
associated with ADC as well as DAC?
a) Analog side to analog ground
b) Digital side to digital ground
c) Use of separate power supply and connection of their ground leads to single point
reference
d) Reduction of inductive loop area between power and return traces [ ]
10. Which among the below stated devices/equipments are preferred for elimination
of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?
a) Coupling capacitor
b) Decoupling capacitor
c) Snubber circuits
d) All of the above
11. Which among the below specified condition is precise in the crosstalk verification
mechanism using logic flow in opposite direction with the limit of avoiding dangerous
interference in digital PCB designing?
a) $Z_{\text{even}} > Z_{\text{odd}}$
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$
c) $Z_{\text{odd}} \ge 0.8 Z_{\text{even}}$
d) $Z_{\text{odd}} = Z_{\text{even}}$
12. Which terminology of PCB represents a thin photo-sensitive polymer by supporting
photographic pattern of single traces or IC pads for etching?
a) Prepreg
b) Etching
c) Photo-resist
d) Solder mask
13. Which problems are about to occur if PCB is not designed properly in a confined
manner for digital circuits?
A. Diffraction
A. Diffraction B. Refraction
B. Refraction C. Ground & Supply-line Noise
B. Refraction C. Ground & Supply-line Noise
B. Refraction C. Ground & Supply-line Noise
B. Refraction C. Ground & Supply-line Noise D. Electromagnetic Interference

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# To F

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Department of Electronics and Communication Engineering

b) B & C	
c) C & D	
d) A, B, C, D	
14. Which type of solderability testing is carried out for the generation of sold	ler sample
due to immersion of wire or sheet metal specimen in a bath of molten solder?	
a) Solder Bath Testing	
b) Meniscus Rise Testing	
c) Solder Iron Testing	
d) None of the above	[]
15. Which among the following assists in obtaining the desired value of wave	impedance
in reflection phase while designing digital PCBs?	
A. Width of signal lines	
B. Distance between signal line and ground line	
C. Signal Delays	
D. Double Pulsing	
a) A & B	
b) B & C	
c) C & D	
d) A, B, C, D	[]
16. What should be the resistance of 0.6 mm wide conductor with 15 cm leng	th and 25
$\mu$ m thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$ (at 20° C)	
a) 118.2 mΩ	
b) 138.2 mΩ	
c) 172.4 mΩ	
d) 192.4 m $\Omega$	[]
17. The actual cost of PCB can be evaluated on the basis of	
a) PCB size & material	
b) Number of layers	
c) Vias on PCB	
d) All of the above	[ ]
18. Which factors contribute to the occurrence of mechanical stress?	
a) Resonance	
b) Cracked Solder Joints	
c) Both a and b	
d) None of the above	[]
19. Which type of PCB requires minimum soldering on component side in or	der to avoid
replacement oriented difficulties?	
a) Single-sided PCB	
b) Double-sided PCB	
c) Both a and b	
d) None of the above	

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Department of Electronics and Communication Engineering

20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

- a)The use of a 3D component
- b) The use of a 3D component and component clearance rule
- c) The use of a courtyard
- d)The use of a courtyard and a component clearance rule

[]

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#### SATES SATES

#### **ANSWERS**

1. Answer: Convection

2. Answer: Electrical Soldering

3. Answer: All of the above

4. Answer: Both a and b

5. Answer: Decrease in the distance between conductors

6. Answer: Removal of heat

7. Answer: SON

8. Answer: Reduction in self-inductance

9. Answer: Reduction of inductive loop area between power and return traces

10. Answer: Decoupling capacitor

11. Answer:  $Z_{odd} \ge 0.8 Z_{even}$ 

12. Answer: Photo-resist

13.Answer: C & D

14. Answer: Meniscus Rise Testing

15.Answer: A & B

16.Answer: 172.4 Mω

17. Answer: All of the above

18. Answer: Both a and b

19.Answer: Double-sided PCB

20. Answer: The use of a courtyard and a component clearance rule

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Department of Electronics and Communication Engineering

Certificate Program on PCB Design Model Question Paper

IVI.	oder Question i aper		
Branch/Sem: II ECE/I SEM Name of the Student: 4. G. G. 7.	ia i	 ROLL Number: <b>218B1A</b> 0	04-75
1. Which phenomenon is not reduced provided by power and return planes a) Radiation	by the circuit paths of l		y
<ul><li>b) Convection</li><li>c) Noise</li><li>d) Crosstalk</li><li>2. Which among the below stated so</li></ul>	oldering methods is also	[ <i>は</i> ] renowned as 'High Frequen	cy
Resistance Soldering'? a) Iron Soldering b) Furnace Soldering			
<ul><li>c) Torch Soldering</li><li>d) Electrical Soldering</li><li>3. Which among the below mention</li><li>Testing?</li></ul>	ed approaches belongs to	o the category of In-circuit	V
a) Impedance Testing			
b) Component Testing c) Apply Signal and check output		ich.	V
d) All of the above 4. What is/are the necessity/ies to p	rovide guarding to precis	sion differential amplifiers?	
<ul><li>a) To increase leakage resistance</li><li>b) To reduce capacitance between s</li></ul>	ignal conductors & grou	nd	
c) Both a and b d) None of the above 5. Which among the below mention	ned assertions is not a wa	[C] ay of cross-talk reduction	
while designing digital PCBs?  a) Decrease in the distance between b) Shielding of clock lines with gua c) Reduction in the loop area of circ	ard strips		
<ul><li>d) Avoid running of parallel traces signals</li><li>6. High current circuits are purpose</li></ul>	for longer distances espe	<i>a</i>	V
accordance to the supply lines for a) Removal of heat			
b) Isolation of stray current c) Reduction of path length			1/
d) All of the above			

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7. Which among the below mentioned packages does not belong to the category o	f 'Small
Outline Package'?	
a) SO	
b) SOP	
c) SOT	[0]
<ul><li>d) SON</li><li>8. What effects can be observed if the separate power and ground planes are provided.</li></ul>	ded
with large conducting surfaces for better decoupling in PCB layouts?	
a) Increase in self-inductance	
b) Reduction in self-inductance	
c) Stability in self-inductance	/
d) None of the above	[6]
9. Which among the below specified assertions is not a grounding consideration	V
associated with ADC as well as DAC?	
a) Analog side to analog ground	
b) Digital side to digital ground	•
c) Use of separate power supply and connection of their ground leads to single po	int
reference	roti /
d) Reduction of inductive loop area between power and return traces	
10. Which among the below stated devices/equipments are preferred for eliminating	)
of ground and supply line noise especially in TTL/CMOS / ECL PCB designing(a) Coupling capacitor	
b) Decoupling capacitor	
c) Snubber circuits	/
d) All of the above	16V
11. Which among the below specified condition is precise in the crosstalk verification.	ation
mechanism using logic flow in opposite direction with the limit of avoiding dang	erous
interference in digital PCB designing?	[C] V
a) $Z_{\text{even}} > Z_{\text{odd}}$	
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$	
c) $Z_{\text{odd}} \ge 0.8 Z_{\text{even}}$	
d) $Z_{\text{odd}} = Z_{\text{even}}$	- autim a
12. Which terminology of PCB represents a thin photo-sensitive polymer by supp	oorung
photographic pattern of single traces or IC pads for etching?	
a) Prepreg b) Etching	
c) Photo-resist	
d) Solder mask	[C] \/
13. Which problems are about to occur if PCB is not designed properly in a conf	
manner for digital circuits?	
A. Diffraction	
B. Refraction	
C. Ground & Supply-line Noise	
D. Electromagnetic Interference	[a] X
a) A & B	1
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b) B & C		
c) C & D		
d) A, B, C, D		
14. Which type of solderability testing is carried	out for the generation of solder sample	
due to immersion of wire or sheet metal specime	n in a bath of molten solder?	
a) Solder Bath Testing		
b) Meniscus Rise Testing		1
c) Solder Iron Testing	(	/
d) None of the above	[6]	
15. Which among the following assists in obtaining	ing the desired value of wave impedance	
in reflection phase while designing digital PCBs	?	
A. Width of signal lines		
B. Distance between signal line and ground line		
C. Signal Delays		
D. Double Pulsing		
a) A & B		
b) B & C		
c) C & D		1
d) A, B, C, D	[a] \	
16. What should be the resistance of 0.6 mm wid		
μm thickness of standard copper foil? (Assume μ	$p = 1.7241 \times 10^{-6} (at 20^{\circ} C)$	
a) 118.2 mΩ		
b) 138.2 mΩ		
c) 172.4 mΩ		1
d) 192.4 mΩ		V
17. The actual cost of PCB can be evaluated on	the basis of	
a) PCB size & material		
b) Number of layers		1
c) Vias on PCB	f and t	/
d) All of the above	[4]	_
18. Which factors contribute to the occurrence of	of mechanical stress?	
a) Resonance		
b) Cracked Solder Joints		
c) Both a and b	r & 1	1
d) None of the above		
19. Which type of PCB requires minimum solde	ering on component side in order to avoid	
replacement oriented difficulties?		
a) Single-sided PCB		
b) Double-sided PCB		/
c) Both a and b	re 1	/
d) None of the above	[6] L	/

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20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

a) The use of a 3D component

b) The use of a 3D component and component clearance rule

c) The use of a courtyard

d)The use of a courtyard and a component clearance rule

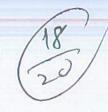
[0]

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Certificate Program on P Model Question P	
Branch/Sem: II ECE/I SEM	ROLL Number: 218B1A0408
Name of the Student: D. Pulitha	ROLL Number 2/86/10408
1. Which phenomenon is not reduced by the circuit provided by power and return planes for shielding pa) Radiation b) Convection	paths of lowest impedances especially ourposes?
c) Noise	
d) Crosstalk	[b] V
<ul><li>2. Which among the below stated soldering method</li><li>Resistance Soldering'?</li><li>a) Iron Soldering</li></ul>	s is also renowned as 'High Frequency
b) Furnace Soldering	
c) Torch Soldering	edi . /
d) Electrical Soldering	
3. Which among the below mentioned approaches b	belongs to the category of in-circuit
Testing?	
a) Impedance Testing	
-b) Component Testing	
c) Apply Signal and check output	1 1
d) All of the above	is a differential amplificate?
4. What is/are the necessity/ies to provide guarding	to precision differential amplifiers?
a) To increase leakage resistance	P. C.
b) To reduce capacitance between signal conductor	's & ground
c) Both a and b	[c] V
d) None of the above	L 3
5. Which among the below mentioned assertions is	not a way of cross-talk reduction
while designing digital PCBs?	
a) Decrease in the distance between conductors	
b) Shielding of clock lines with guard strips	
c) Reduction in the loop area of circuits	and a second like for a symphesis
d) Avoid running of parallel traces for longer dista	nces especially for asynchronous
signals	a V
6. High current circuits are purposely located or pl	aced near the edge of PCB III
accordance to the supply lines for	
a) Removal of heat	
b) Isolation of stray current	
c) Reduction of path length	[I-] ×
d) All of the above	[6] X

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Department of Electronics and Communication Engineering

_		_	
	7. Which among the below mentioned packages does not belong to the category of	''Sma	all
	Outline Package'?		
	a) SO		
	b) SOP		
	c) SOT	r - 47	1/
	d) SON	[0]	
	8. What effects can be observed if the separate power and ground planes are provided in the separate power and ground planes are provided	ied	
	with large conducting surfaces for better decoupling in PCB layouts?		
	a) Increase in self-inductance		
	b) Reduction in self-inductance		
	c) Stability in self-inductance		
	d) None of the above	[6]	V
	9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?		
	a) Analog side to analog ground		
	b) Digital side to digital ground		
	c) Use of separate power supply and connection of their ground leads to single poir reference	nt	
	d) Reduction of inductive loop area between power and return traces	[d]	. /
	10. Which among the below stated devices/equipments are preferred for elimination		V
	of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?	)11 	
	a) Coupling capacitor	6	
	b) Decoupling capacitor		
	c) Snubber circuits		
	d) All of the above	Mal	^
	11. Which among the below specified condition is precise in the crosstalk verifica	[6]	V
	mechanism using logic flow in opposite direction with the limit of avoiding dange		
	interference in digital PCB designing?		./
		[C]	V
	a) $Z_{\text{even}} > Z_{\text{odd}}$		
	b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$		
	c) $Z_{\text{odd}} \ge 0.8 Z_{\text{even}}$		
	<ul> <li>d) Z<sub>odd</sub> = Z<sub>even</sub></li> <li>12. Which terminology of PCB represents a thin photo-sensitive polymer by support</li> </ul>	ortina	
	photographic pattern of single traces or IC pads for etching?	JITHE	3
	a) Prepreg b) Etching		
	c) Photo-resist	[C]	./
	d) Solder mask		
	13. Which problems are about to occur if PCB is not designed properly in a confirmation of the designed properly in the design of the desi	iea	
	manner for digital circuits?  A. Diffraction		
	B. Refraction  C. Graund & Supply line Naise		
	C. Ground & Supply-line Noise	[0]	. 1
	D. Electromagnetic Interference	[a]	X
	a) A & B		1
	100000		
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b) B & C		
c) C & D		
d) A, B, C, D		
14. Which type of solderability testing is carried out for the generation of solde	r sample	
due to immersion of wire or sheet metal specimen in a bath of molten solder?		
a) Solder Bath Testing		
b) Meniscus Rise Testing		
c) Solder Iron Testing		1
d) None of the above	[6]	V
15. Which among the following assists in obtaining the desired value of wave i	mpedance	
in reflection phase while designing digital PCBs?		
A. Width of signal lines		
B. Distance between signal line and ground line		
C. Signal Delays		
D. Double Pulsing		
a) A & B		
b) B & C		
c) C & D		
d) A, B, C, D	[a] 1	
16. What should be the resistance of 0.6 mm wide conductor with 15 cm length	1 and 25	
$\mu$ m thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6}$ (at 20° C)		
a) 118.2 mΩ		
b) 138.2 mΩ		
c) 172.4 mΩ		/
d) 192.4 mΩ	[C] L	
17. The actual cost of PCB can be evaluated on the basis of		
a) PCB size & material		
b) Number of layers		
c) Vias on PCB		
d) All of the above	[d]	1
18. Which factors contribute to the occurrence of mechanical stress?		
a) Resonance		
b) Cracked Solder Joints		
c) Both a and b		1
d) None of the above	[C]	V
19. Which type of PCB requires minimum soldering on component side in ord	er to avoid	
replacement oriented difficulties?		
a) Single-sided PCB		
b) Double-sided PCB		
c) Both a and b	F 4.3	/
d) None of the above		

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20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

a)The use of a 3D component

- b) The use of a 3D component and component clearance rule
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- d)The use of a courtyard and a component clearance rule

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## Certificate Program on PCB Design Assessment Marks

A.Y: 2022-2023 Year: II

S. No	Reg. No	Name of the Candidate	Marks
1	218B1A0401	BANDARU AKHILA	19
2	218B1A0402	BODEY SEETHA MAHALAKSHMI	18
3	218B1A0403	BOMMISETTY NAGA NIKITHA	17
4	218B1A0404	CHAPPIDI SUPRITHA	18
5	218B1A0405	VALLAMSETTI VENKATA NAGA ANUSHA	17
6	218B1A0406	DARSI SWATHI	18
7	218B1A0407	DHUPATI KAVITHA	19
8	218B1A0408	DIVVELA PUJITHA	18
9	218B1A0409	DUPATI APARNA	18
10	218B1A0410	GIDDA ANJALI	17
11	218B1A0411	GOGINENI DEEPTHI	19
12	218B1A0412	GOSU JAYA SRI	20
13	218B1A0413	KARIDHU KALYANI	20
14	218B1A0415	KOKKILIGADDA BHAVANI	16
15	218B1A0416	KONIKI POOJITHA	. 19
16	218B1A0417	KONIKI PRAVALLIKA	16
17	218B1A0418	MANNEM DEEPIKA JYOTHI	20
18	218B1A0419	MURAKONDA VENKATA JASMITHA	16
19	218B1A0420	NARIPEDDI VENKATASIVANAGARAJA	19
20	218B1A0421	NELAPATI VYSHNAVI	18
21	218B1A0422	PABOLU APARNA	19
22	218B1A0423	PAVANI ANUPRAVALLIKA	18
23	218B1A0424	PILLI AMMULU	17
24	218B1A0425	POKURI NANDINI	17
25	218B1A0426	REVURI VIJITHA	17
26	218B1A0427	SHAIK KARISHMA	19
27	218B1A0428	SHAIK SHIRAJ UNNISA BEGUM	16
28	218B1A0429	SYED NOORI	19
29	218B1A0430	TENALI AMULYA	19
30	218B1A0432	AKULA MOHAN VAMSI NADH	20
31	218B1A0433	ALAHARI RAMESH	17
32	218B1A0434	DAMA MANIKNTA	18
33	218B1A0435	ANUMALA PRAVEEN	18
34	218B1A0436	ARIBOYINA DHARMA TEJA	19

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Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
35	218B1A0437	BOGISETTY PREMCHAND	17
36	218B1A0438	BOTTU YASWANTH	18
37	218B1A0439	CHAVATAPALEM SIVA SANKAR	17
38	218B1A0440	CHILAKAPATI SHANMUKHA SAI RAM	18
39	218B1A0441	CHINNAPUREDDY KOTIREDDY	19
40	218B1A0442	DEVARAPALLI HARSHAVARDHAN	18
41	218B1A0443	ENUGU HARSHAVARDHAN	18
42	218B1A0444	GADDALA ISSAKU	18
43	218B1A0445	GUNJI ACHYUTH	19
44	218B1A0446	KALAPALA SIVARAMABRAHMACHARI	18
45	218B1A0447	KANTA GOVINDAIAH	19
46	218B1A0448	KATTA SASI KUMAR	19
47	218B1A0449	KOKKILAGADDA ASHOK KRISHNA	20
48	218B1A0450	KOTA DINESH	16
49	218B1A0451	MEDAM HARSHITH	19
50	218B1A0452	LAKKAMRAJU ADI SANKARA NARAYANA RAJU	18
51	218B1A0453	LAKKIREDDY VEERA VENKATA PRATHAP REDDY	19
52	218B1A0454	MULE VENKATESWARLU	17
53	218B1A0456	PASAM NAVEEN	19
54	218B1A0457	PATAN SALLAUDDIN	16
55	218B1A0458	PILLI BRAHMA REDDY	18
56	218B1A0459	PUTTA NAVINESH REDDY	18
57	218B1A0460	PUVVADA YASHWANTH KUMAR	18
58	218B1A0461	SHAIK JANIBASHA	15
59	218B1A0462	SHAIK MUNEER AHAMAD	19
60	218B1A0463	SHAIK SAMEER	18
61	218B1A0464	SWARNA GOPI	19
62	218B1A0465	TANGUTURI PAVAN KUMAR	17
63	218B1A0466	UPPALAPATI SRINU	19
64	218B1A0467	ELAPALAPATI NAVYA TEJA	16
65	218B1A0468	ALAHARI SRI PRIYANKA	16
66	218B1A0469	BANDELA SANJAMMA	16
67	218B1A0470	BAPIREDDY SNEHA LATHA	17
68	218B1A0471	BOLLAVARAM SHREYA	15
69	218B1A0472	DASARI NANDINI	18
70	218B1A0474	GADDALA SUBHASHINI	17
71	218B1A0475	INDLA GIRIJA	19

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Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
72	218B1A0476	JASTI SIREESHA	17
73	218B1A0477	KAMASANI ANUSHA	18
74	218B1A0478	KODURI SIRISHA	17
75	218B1A0479	KONDURI PUJITHA REDDY	18
76	218B1A0480	KOTTURI GAYATHRI	19
77	218B1A0481	KUKATLA AMULYA	18
78	218B1A0482	KUMMITHA AMULYA	18
79	218B1A0484	MALIREDDY CHANDU PRIYA	17
80	218B1A0485	MEDIKONDA MANISHA	19
81	218B1A0486	MIDASALA PRAVALLIKA	20
82	218B1A0487	NALAGANGA PRAVALLIKA	20
83	218B1A0488	NALLABOTHULA SULOCHANA	20
84	218B1A0489	NALLURI KAVYA	20
85	218B1A0490	ORCHU DURGA	20
86	218B1A0491	PATAN ISHRATH	17
87	218B1A0492	PERAM VENKATA SALVANI	19
88	218B1A0493	POKURU LAKSHMI SOWJANYA	18
89	218B1A0494	RASIM LAKSHMI BHAVANI	19
90	218B1A0495	REDITHI AKSHAYA	19
91	218B1A0496	SANNEBOINA THULASI	19
92	218B1A0497	SANNEBOYINA SRI LAKSHMI	19
93	218B1A0498	SOMINENI AMULYA	19
94	218B1A0499	SURA ANUSHA	19
95	218B1A04A0	SURAM NANDINI	19
96	218B1A04A1	UDAYAGIRI CHENCHAMMA	19
97	218B1A04A2	UTUKURI KALYANI	18
98	218B1A04A3	VELUGOLU VENKATA ANANTHA LAKSHMI	18
99	218B1A04A4	YARAM ANKITHA	16
100	218B1A04A5	YENIMIREDDY VINEELA	19
101	218B1A04A6	ATHANTY ARUN KUMAR	19
102	218B1A04A7	AVVARU VENKATA GANESH	20
103	218B1A04A8	BATHINA AKHIL	18
104	218B1A04A9	DANDEBOYINA MAHESH	20
105	218B1A04B0	DHARNASI RAKESH	20
106	218B1A04B1	GUDLURU BHANUPRAKASH	19
107	218B1A04B2	KAKARLA MANOHAR	19

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Department of Electronics and Communication Engineering

S. No	Reg. No	Name of the Candidate	Marks
108	218B1A04B3	KAKUNURI VENKATA DURGA PRASAD REDDY	19
109	218B1A04B4	KALLURI DINESH BABU	19
110	218B1A04B5	KASU RADHAKRISHNA	18
111	218B1A04B6	KAVURI BALA VIGNA MANI KANTA	19
112	218B1A04B7	KONIKI SHIVAJI	18
113	218B1A04B8	KURRA BALARAJU	16
114	218B1A04B9	ERISETTY SRINIVASULU	17
115	218B1A04C0	MASUNURI VENKATA KASI NAGA MANIKANTA	16
116	218B1A04C1	MEDAM VENKATA VISHNU VARDHAN REDDY	16
117	218B1A04C2	PODILI VEERA HANUMA	15
118	218B1A04C3	SHAIK AYAAZ	18
119	218B1A04C4	THATIKONDA VENKATA VAMSI	17
120	218B1A04C5	THOKA KARUNAKAR	19
121	218B1A04C6	YADLA MADESH REDDY	19
122	228B5A0401	AYINAMPUDI GIREESH KUMAR	19
123	228B5A0402	CHEREDDY SUBRAHMANYAM	20
124	228B5A0403	MANGOLLU NIKHILA	20
125	228B5A0404	RAVULAPALLI AMARNADH	20
126	228B5A0405	SINGAMREDDY MALYADRI	15
127	228B5A0406	VELUGOLU VIKAS	16
128	228B5A0407	APPADI RAJ KUMAR	15
129	228B5A0408	GOLLAPOTHU YASWANTH	15
130	228B5A0409	RAYANA PAVAN KUMAR	18
131	228B5A0410	TANNIRU HARSHA VARDHAN	18
132	228B5A0411	KOPPARTHI AKHIL	19

Doordinator

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HEAD OF THE DEPARTMENT
Department of E.C.E.
RISS Krishna Sai Gandhi Group
RISS Krishna Sai Gandhi Group

PRINCIPAL

RISE KRISHNA SAI GANDHI

## RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS: ONGOLE DEPARTMENT OF ECE

[Certificate program on PCB Design 14-11-2022 to 18-11-2022]

The Certificate Program conducted by ECE department on 14th - 18th Nov - 2022 in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS in association with Center for Electronics System Design (CESD)

Department of Electronics & Communication Engineering



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#### Objectives of conducting Certificate program

- To make students learn and interact with renowned industry experts.
- Make Students to receive an unparallel education on the art of PCB Designing Certificate program with personal one on one attention.
- To make every student an expert in designing their own PCB board which would be very useful for developing their own projects.

#### Overview about Certificate Program:

The aim of this **Certificate Program** is to make the students learn the designing and manufacturing of a printed circuit board using open source KICAD PCB design software and with various active and passive components such as Regulators, Diodes, Resistors, Capacitors, Inductors, Switches, e.t.c.

#### **Technical Support:**

The Certificate Program was conducted in collaboration with Center for Electronics System Design (CESD) from Vijayawada. The company has a fast growth in PCB designing. The company's director Mr. Finney Daniel accompanied with Seven Trainers attended the Certificate Program for guiding the students in learning the technologies of the PCB Design Certificate Program. They have taken about 32 hours of theoretical and practical sessions.

#### Department of ECE:

Department of ECE has taken the opportunity to conduct the in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS. As the theme of the Certificate Program is the core for the department, it's a nice opportunity for the students to learn the technology and to implement that practically.

#### Technical Report on Certificate Program:

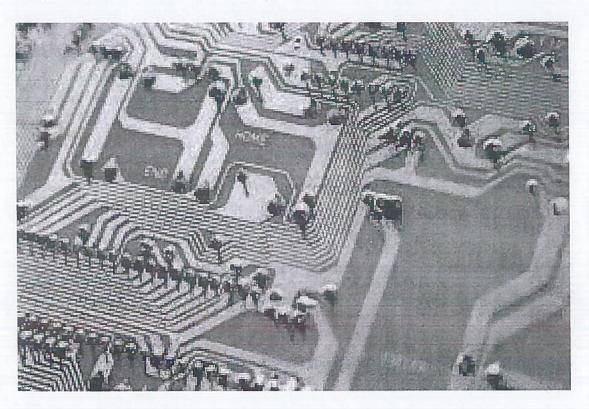
The Technical team of Center for Electronics System Design (CESD) has described the entire designing process in a step by step procedure.

#### 1. Basic PCB Concepts

First of all they have given the concepts which will be very helpful for designing the PCB practically, using some power point presentations. In this theoretical explanation part they have explained about the KI-CAD software and the use of software for further practical implementation in designing the PCB. They have also

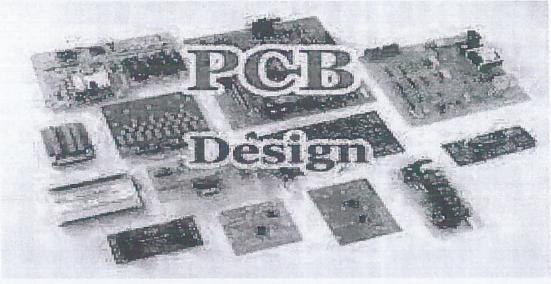


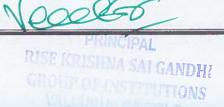
given a briefing about active and passive electronic components which they will be using in a PCB.



### 2. Editing and Routing

Editing and Routing is the basic step and it is one of the important step for designing a PCB. Editing and Routing gives the circuit layout from one component to the other components. Soldering plays a key role in this step.





#### 3. Creation of Library and Components & Report Generation

This is a step done using KI-CAD tools. In this step the components in the circuit and the respective libraries are selected in this software. So that the required circuit will be designed in the software and a print of the same will be taken on a sheet. The same print will be useful for the further process.

#### 4. Toner Transfer Method

This is the step where the designed circuit will be pasted on the wafer and this will be passed through a temperature of about 160 to 180 degrees so that the tracks of the circuit will be remained on the wafer. The tracks will be a conductive type.

#### 5. Drilling Technique

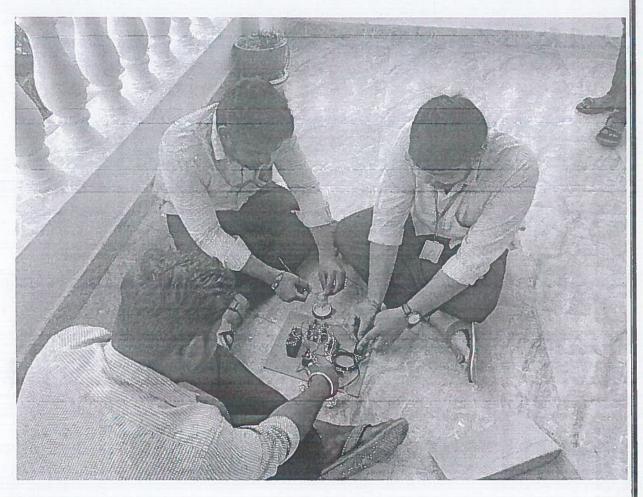
The board will be drilled with holes where the components have to be placed; the holes will be drilled in the board depending on the terminals available for the components in the design. The hole should be in the size so that the terminal has to be freely placed in the hole.

#### 6. Soldering Technique

The components that are placed in the board should be soldered to the track so that the circuit is connected as per the design. After this step the engraved PCB will be ready to use.

The Department conducted test on PCB Design for Electronic components and all project models are exhibited in the respected department

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#### Student Response

Almost 132 students had taken part in the Certificate Program. All the students responded that they have learned and had hands on experience in designing a PCB. They are very excited in participation in this Certificate Programand requested for more Certificate Program in similar way so that they can simultaneously gain the practical knowledge.

#### Distribution of Certificates

At the last day question answer session and certificate distribution function started on 4:30 PM. Feedbacks regarding workshop are provided by various students.

All the students were awarded with a participation certificate from the company Center for Electronics System Design (CESD). Principal Dr.K.V.Subrahmanyam garu awarded the certificates to all the students by hand. He personally congratulated every student for participating in the event and making it successful.

RISE KRISHNA SAI GANDHI

#### Vote of Thanks

Mr.S V Ravi Kumar beloved HOD of ECE Department thanked every student for their active participation and interest in participating in the Certificate Program and mentioned about the activities conducted in the college by the department. He promised that department will continue its assistance in conducting these sorts of Certificate Programs and seminars in future.

He thanked the technical support given by **Center for Electronics System Design (CESD).** He personally felt very happy for the response of the company and satisfied with the way they conducted the Certificate Program.

He mentioned about the marvelous support given by the Principal Dr.K.V.Subrahmanyam garu to the department in conducting these Certificate Program. He also thanked for the personal interest taken by him in encouraging the department in all aspects.

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NH-16, Valluru, Ongole, Prakasam (District)-523272

Deportment of Electronics and Communication Engineering

Department of Electronics and Communication Engineering

Date: 18-11-2022.

#### **CLOSING REPORT**

To, The Principal, RISE Krishna Sai Gandhi Group of Institutions.

As per the approved schedule, the ECE department has conducted a Certificate Program on "PCB Design" at ECE Seminar hall from 14-11-2022 to 18-11-2022. 132 students of II ECE have participated in this program. Sri **F.Daniel**, Director, Center for Electronics Systems Design (CESD), Vijayawada, AP, acted as the resource person for this program.

Main issues addressed:

- 1. Basic PCB Concepts
- 2. Editing and Routing
- 3. Creation of Library and Components & Report Generation
- 4. Toner Transfer Method
- 5. Drilling Technique
- 6. Soldering Technique

We are expecting your support in future also. Thanking you sir,

Yours faithfully,

S.V. doni

Department of E.C.E.
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