Department of Electronics and Communication Engineering



Certificate Program

On

"PCB Design "

Date: 22ndto 26th March 2021

Finney Daniel

Dirctor,center for electronics system design Vijayawada

PRINCIPAL

RISE KRISHNA SAI GANDHI

GROUP OF INSTITUTIONS

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(Approved by AICTE, New Delhi & Affiliated to JNTUK, Kakinada) NH-16, Valluru, Ongole, Prakasam (District)-523272

Valluru,

Date: 02-03-2021

To

F.Daniel, Dirctor, Center for Electronics System Design, Vijayawada.

Dear Sir,

Subject: Inviting for Certificate program - Reg.

Greetings from RISE Krishna Sai Gandhi Group of Institutions, Ongole

As per the discussion with Dr.K.V.Subrahmanyam, Principal, of our Institute, I hereby take this opportunity to invite you to conduct the Certificate program on **PCB Design** "From 22-03-2021 to 26-03-2021.

You are requested to interact and provide guidance to our II B.Tech students, who are looking forward to their bright career ahead. I will feel honored by your gracious presence at our organization. I believe that your lecture will help our students and faculty members to explore knowledge.

Thanking you in anticipation.

Yours sincerely,

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GROUP OF INSTITUTIONS

VALLURU: ONGOLE.

No. of Contract of

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VALLURU:: ONGOLE.

Finney Daniel

Managing Director
Center for Electronics System Design

Personal Summary

Finney Daniel has a record of organizing Institutional Industry oriented up-gradation programs for undergraduates. Experienced in delivering recent trend technologies to the personnel in vivid methodologies. Providing a lawn of possibilities in the specified area which strengthen the personnel in growing the skills required for their success in the present day competence. He has experience as a guest lecturer, assistant professor and a research fellow. His main interest in this has been to prove the potential and ability of the personnel.

Professional Summary

- Delivered services as Guest Lecturer for VLSI in Andhra University College of Engineering.
- Worked as Assistant Professor in couple of Engineering Colleges.
- As Junior Research Fellow in Defence Research & Development Laboratory.

Areas of Expertise

- **Product Development:** Evolving modules that enable a final product meeting the End- User requirements and facilitate easy utility of the product
- Project Management: Maintaining strategic planning and supporting the team in delivering Robust Models by providing employ friendly platform.
- Organizing Training Sessions: Planned tabulation for training and hands on expertise for the personnel under training.

Professional Skills and Competencies

- Strong knowledge on Software tools like QUARTUS, Xilinx, Cadence, Tanner- EDA, Mentor-Graphics required for VLSI.
- Good knowledge on hardware design and development includes familiarity in Embedded System tools and PCB design tools like MPLAB Xpress IDE, KEIL, Micro-c, ZUKEN- Cadstar, Eagle, Express-PCB.

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AND LATUTIONS

Key Roles

- Academic Director for KR's Educational Society.
- Coordinator for Technical Symposium in Holy Mary Group of Institutions.
- Organized Workshops on Verilog, PCB Design, Prototyping, Embedded Systems, Product Design and Development.

Qualification

- Master of Technology in VLSI-System Design from JNTU-Kakinda.
- PG Diploma in Electronic Product Design from Electronics System Design and Manufacturing (ESDM, Govt. of India).
- Graduation in Electronics & Communication Engineering from CJITS, JNTU- Hyderabad.
- Graduation in Bachelor of Science in Mathematics from Andhra University.

Personal Details

- Born on 21[№] June 1987 in Visakhapatnam.
- Indian citizen and can speak Hindi, English, Telugu.

References - Available on Request.

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PROPOSAL FORM

SUB: Certificate program - Program.

TO THE SECRETARY/CORRESPONDENT THROUGH PRINCIPAL FOR KIND APPROVAL

1	NAME OF THE INSTITUTION	Rise Krishna Sai Gandhi Group of Institutions
2	NAME OF THE DEPARTMENT	Electronics & Communication Engineering
3	TITLE OF THE PROGRAMME	Certificate program
4	NAME OF THE PROGRAMME	Certificate program on "PCB Design for Electronic Designs"
5	OBJECTIVE OF THE PROGRAMME	To bring the exposure in the PCBDesign.
6	DETAILS OF RESOURCE PERSON(S)& CV ATTACHED.	Finney Daniel Director, center for electronics system design Vijayawada.
7	PROPOSED DATE(S)/ACADEMIC YEAR	22-03-2021 to 26-03-2021
8	DURATION OF THE PROGRAMME	FIVE DAY
9	VENUE	Seminar Hall
10	TARGETS	II ECE students
11	No. OF PARTICIPANTS	65 Students
12	REGISTRATION FEE	Free
13	NAME OF PROGRAMME CO ORDINATOR(S)	Mr. K.Nagahanuma Chari
14	NAME OF THE STUDENTS COORDINATOR(S)	1.Mr. MadalaAmarnath (198B1A0450) 2.Ms.Kunchala Akhila(208B5A0401)

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Department of Electronics and Communication Engineering

15	SOURCE OF FUND IDENTIFIED	Management
16	MANAGEMENT CONTRIBUTION REQUIRED	YES
17	PROPOSAL PREPARED BY	Mr.K.Nagahanuma Chari (CO-ORDINATOR)

S.N. 000 &

HEAD OF THE DEPARTMENT Department of E.C.E. RISE Krishna Sai Gandhi Group of Institutions, VALLURU, A.P.-523 272

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NH-16, Valluru, Ongole, Prakasam (District)-523272

Department of Electronics and Communication Engineering

Valluru, Date: 19-03-2021.

CIRCULAR

This is to inform II B.Tech students and faculty that there will be a 5-Day Certificate program on "PCB Design" from 22-03-2021 to 26-03-2021 by F.Daniel, Director, Center for Electronics System Design, Vijayawada.

Copy to:

Principal

Staff Circular

Students of ECE II year

ECE Department Notice Boards

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HEAD OF THE DEPARTMENT Department of E.C.E. RISE Krishna Sai Gandhi Group of Institutions, VALLURU, A.P.-523 272

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Certificate Program on "PCB Design"

Date: 22nd to 26th Mar 2021

SCHEDULE FROM 22-03-2021 TO 26-03-2021

S. No	Program List	Tim	ing
		From	То
	DAY - 01 (22-03-20	021)	
1	Program started	09.00 AM	,
2	Lamp lighting	09.00 AM	09.10 AM
3	Principal speech	09.10 AM	09.25 AM
4	HOD Introduction about PCB Design	09.25 AM	09.35 AM
5	Tea Break	09.35 AM	10.00 AM
6	Introduction about PCB concepts	10.00 AM	01.00 PM
7	Lunch Break	01.00 PM	01.45 PM
8	KI-CAD Software Practical Section	01.45 PM	05.00 PM
	DAY - 02 (23-03-2	021)	
9	Concepts of PCB Designing, PCB Materials, Layers	09.00 AM	12.15 PM
10	Lunch Break	12.15 PM	01.00 PM
11	Multilayer Concepts	01.00 PM	05.00 PM
	DAY - 03 (24-03-2	021)	
12	PADSTACK	09.00 AM	12.15 PM
13	Lunch Break	12.15 PM	01.00 PM
14	Schematic entry KI-CAD tools	01.00 PM	05.00 PM
	DAY - 04 (25-03-2	021)	
15	Drawing a schematic FLAT	09.00 AM	12.15 PM
16	Lunch Break	12.15 PM	01.00 PM
17	BOM. Net list generation	01.00 PM	05.00 PM
	DAY - 05 (26-03-2	021)	
18	Designing Boards	09.00 AM	12.15 PM
19	Lunch Break	12.15 PM	01.00 PM
20	Drawing a schematic HIERARCHICAL Design	01.00 PM	04.15 PM
21	Certificate Program Exam	04.15 PM	04.45 PM
22	Vote of Thanks	04.45 PM	05.00 PM

Coordinator

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RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Student: Challa. Thiven

Roll No : 19881A0405
Topic : Certificate Program on "PCB Design"

Date: 26-03-2021

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?		/			
2	Is the certification program well planned or not?		1			
3	Lecture makes objectives clear?			THE STATE OF		
4	Lecture speaks clearly and audibly?		1			
5	Lecture explains with exaples clearly?		/			
6	Is you are doubts clarified or not?					

5-Excellent

4-Good

3-Average

2-Poor

1- No comment

PRINCIPAL



RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OI LECTRONICS AND COMMUNICATION ENGINEE

Student Feedback Form

Name of the Student: Dumpa Sandhya

Roll No : 19881A0415
Topic : Certificate Program on "PCB Design"

Date: 26-03-2021

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?		/			
2	Is the certification program well planned or not?	1				
3	Lecture makes objectives clear?	/	,			-
4	Lecture speaks clearly and audibly?		/			
5	Lecture explains with exaples clearly?	1				
6	Is you are doubts clarified or not?					

5-Excellent

4-Good

3-Average

2-Poor

1- No comment

VALLURU: ONGOLE.



RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING

Name of the Student: Modispedy . Anuska.

Roll No : 19881A0421

Topic: Certificate Program on "PCB Design"

Date: 26-03-2021

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?		/			
2	Is the certification program well planned or not?					
3	Lecture makes objectives clear?		/			
4	Lecture speaks clearly and audibly?					
5	Lecture explains with exaples clearly?					
6	Is you are doubts clarified or not?					

5-Excellent

4-Good

3-Average

2-Poor

1- No comment

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RISE KRISHNA SAI CANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELL TRONICS AND COMMUNICATION ENGINEERII

Name of the Student: GOOUGOOR ON TO HOST

Roll No : 19881A0443
Topic: Certificate Program on "PCB Design"

Date: 26-03-2021

S.No	Feedback Points	5	4	3	2	1
1	Is the certification program useful or not?	/				
2	Is the certification program well planned or not?					
3	Lecture makes objectives clear?					
4	Lecture speaks clearly and audibly?					
5	Lecture explains with exaples clearly?					
6	Is you are doubts clarified or not?	./				

5-Excellent 4-Good 3-Average 2-Poor

1- No comment

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RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS:: ONGOLE DEPARTMENT OF ELECTRONICS AND COMMUNICATION ENGINEERING CERTIFICATE PROGRAM FEEDBACK ANALYSIS

Date: 26-03-2021

A.Y: 2020-2021 Year: II B.Tech ECE

S.No	Roll Number	Name	1	2	3	4	5	6
1	198B1A0401	APPALA DURGA MAHALAKSHMI	5	4	5	4	5	5
2	198B1A0402	BANDARU DHARANI	5	4	5	4	5	4
3	198B1A0404	BOGALA CHINNAKKA	4	-5	4	5	5	5
4	198B1A0405	CHALLA THRIVENI	4	4	5	4	4	4
5	198B1A0407	CHANDRA UMARANI	5	5	5	4	4	5
6	198B1A0408	CHEMBETI VASANTHI	4	4	5	4	5	5
7	198B1A0410	DANDIBOYINA SRAVANI	4	4	5	4	4	5
8	198B1A0411	DEVARAKONDA NEERAJA	5	4	4	5	5	4
9	198B1A0412	DEVARAMPATI VISHALI	4	4	5	4	4	5
10	198B1A0413	DEVATHA NAGAJYOTHI	4	5	5	4	5	4
11	198B1A0414	DUDDIKUNTA JYOTHI REDDY	4	4	4	4	5	5
12	198B1A0415	DUMPA SANDHYA	4	5	5	4	5	4
13	198B1A0416	EEMANI SWAPNA	4	4	5	4	5 -	5
14	198B1A0417	JAMPANI HARI VANDANA	4	5	5	4	5	5
15	198B1A0418	JYOSHNA VAKA	4	4	5	5	5	5
16	198B1A0419	KONDURI SANTHOSHI POORNIMA	5	5	4	4	5	4
17	198B1A0420	KOTA YAMINI	A 4	5	5	4	5	5

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S.No	Roll Number	Name	1	2	3	4	5	6
18	198B1A0421	MADIREDDY ANUSHA	4	5	4	5	5	4
19	198B1A0422	MANDAPATI SAI PREETHI	4	4	5	5	5	. 5
20	198B1A0424	PADARTHI VENKATA SAI AKHILA	5	5	5	5	5	5
21	198B1A0425	PARIMI SUREKHA	4	5	4	5	5	5
22	198B1A0426	PATHURI ABHINAYA	4	4	5	4	5	4
23	198B1A0427	PUNUGOTI BHULAKSHMI	4	4	5	4	4	5
24	198B1A0428	RAVURI LAKSHMI	5	4	4	4	4	5
25	198B1A0429	SHAIK HUZURUNNISA	5	5	5	5	5	5
26	198B1A0430	SHAIK RUKHYA	5	4	5	4	4	5
27	198B1A0431	TAMALAPAKULA KAVITHA RANI	5	4	5	5	5	4
28	198B1A0432	THATI THOTI PARIMALA	5	5	4	4	4	5
29	198B1A0433	VADLAMUDI DEEPTHI	4	4	5	4	5	5
30	198B1A0434	VEMULA MOUNIKA	5	4	5	4	5	4
31	198B1A0436	ANUMOLU MANIDEEP	5	4	5	4	5	5
32	198B1A0437	BELLAMKONDA DANAMURTHI	5	5	4	4	4	5
33	198B1A0439	CHITIRALA VISHNU VARDHAN	5	5	4	5	4	5
34	198B1A0440	DEPURI HARIKRISHNA	5	4	4	4	5	4
35	198B1A0441	EDAMAKANTI RAVI	5	5	4	5	5	5
36	198B1A0442	GONUGUNTA HARI BABU	5	4	5	4	4	4
37	198B1A0443	GONUGUNTA MAHESH	5	5	5	4	4	5

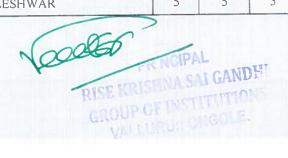
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S.No	Roll Number	Name	1	2	- 3	4	5	6
38	198B1A0444	KANDLAGUNTA NAVEEN KUMAR	5	4	5	4	4	5
39	198B1A0445	KASU DURGA RAJESWAR REDDY	4	5	5	4	4	4
40	198B1A0446	KATIKALA AMITH	5	4	5	4	5	5
41	198B1A0447	KESAMREDDY PRABHAKAR	5	4	4	5	5	5
42	198B1A0448	KUNCHALA ASHOK	5	4	5	5	5	5
43	198B1A0449	KUNCHALA HARESH	5	5	5	5	5	4
44	198B1A0450	MADALA AMARNADH	5	4	4	4	4	5
45	198B1A0451	MADDULURI SIVA SAI KUMAR	5	5	5	5	5	5
46	198B1A0452	MAMILLAPALLI SUMANTH KUMAR	4	5	4	5	4	5
47	198B1A0453	MANNEM MAHESH	5	4	4	4	5	5
48	198B1A0454	MEDIKONDA RAMAKRISHNA	5	5	5	5	5	5
49	198B1A0455	MOLABANTI NAGA SRINU	4	4	5	5	4	4
50	198B1A0456	MUNAGALA CHARAN REDDY	5	4	5	4	5	5
51	198B1A0457	PAMBA ANJAIAH	5	4	5	4	5	5
52	198B1A0458	RAVULAPALLI CHARAN KUMAR	5	4	5	5	5	5
53	198B1A0459	RENUMALA NAGAMUTTHU	5	4	5	4	5	5
54	198B1A0460	SHAIK AZMAL	5	4	5	4	5	5
55	198B1A0461	SHAIK SHAJAHAN	5	4	5	4	5	5
56	198B1A0462	TELUKUTLA GOPI	5	4	4	4	5	5
57	198B1A0463	THANNIRU DURGA MALLESHWAR	5	5	5	4	5	5



S.No	Roll Number	Name	1	2	3	4	5	6
58	198B1A0464	VADDEMPUDI REVANTH	5	5	5	5	5	5
59	198B1A0465	PULI JAYARAMIREDDY	5	5	5	4	5	5
60	208B5A0401	KUNCHALA AKHILA	5	4	4	4	5	5
61	208B5A0402	POTU SRI MOUNIKA	4	4	5	5	4	4
62	208B5A0403	SYED TASNIMKAUSAR	5	4	5	4	5	5
63	208B5A0404	VENNAPUSA ESWAR REDDY	5	4	5	4	5	5
64	208B5A0405	SYED JAFAR	5	4	4	4	4	5
65	208B5A0406	TANNIRU MANOJ KUMAR	5	5	5	5	5	5
			4.68	4.39	4.69	4.39	4.71	4.78
			93.68	87.84	93.73	87.84	94.12	95.69

Your Coordinator

S.N. John &

HEAD OF THE DEPARIMENT
Department of E.C.E.
RISE Krishna Sai Gandhi Group
of Institutions ALLURU A.P. 523 772

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Department of Electronics and Communication Engineering

Certificate program Feedback Analysis

: Certification program on" PCB Design" Topic

Resource Person : F.Daniel

Director, center for Electronics System Design, Vijayawada

: 22-03-2021 to 26-03-2021 Dates

Venue : Seminar Hall

: II Year students Targeted Students

S.No	No. of students Participated	No. of students given feedback	Feedback %
1	65	65	100%

HEAD OF THE DEPARTMENT Department of ECE RISE Krishna Sai Gandhi Group of lastitutions, VALLURU, A.P.-523 272

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Department of Electronics and Communication Engineering

Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM	
Name of the Student:	ROLL Number:
1. Which phenomenon is not reduced by the circuit paths of provided by power and return planes for shielding purpose a) Radiation	flowest impedances especially s?
b) Convection	
c) Noise	
d) Crosstalk	[]
2. At absolute temperature, an intrinsic semiconductor has	
a)A free electrons	
b) Many holes	
c) Many free electrons	
d) No holes or free electrons	
3. Which among the below stated soldering methods is also	o renowned as 'High Frequency
Resistance Soldering'?	
a) Iron Soldering	
b) Furnace Soldering	
c) Torch Soldering	
d) Electrical Soldering	
4. Which among the below mentioned approaches belongs	to the category of In-circuit
Testing?	
a) Impedance Testing	
b) Component Testing	
c) Apply Signal and check output	r 1
d) All of the above	
5. Which type of solderability testing is carried out for the due to immersion of wire or sheet metal specimen in a bat a) Solder Bath Testing	h of molten solder?
b) Meniscus Rise Testing	
c) Solder Iron Testing	
d) None of the above	[]
6. What is/are the necessity/ies to provide guarding to pre	L 3
a) To increase leakage resistance	olston anti-contract and pro-
b) To reduce capacitance between signal conductors & gr	ound
c) Both a and b	
d) None of the above	
d) 140110 of the above	

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7. Which among the below mentioned assertions is not a way of cross-talk reductive while designing digital PCBs? a) Decrease in the distance between conductors b) Shielding of clock lines with guard strips c) Reduction in the loop area of circuits d) Avoid running of parallel traces for longer distances especially for asynchronous signals[] 8. Which among the below mentioned packages does not belong to the category of Outline Package'? a) SO b) SOP	us
c) SOT	
d) SON	
9. Which among the below specified assertions is not a grounding consideration associated with ADC as well as DAC?a) Analog side to analog ground	
b) Digital side to digital ground	
c) Use of separate power supply and connection of their ground leads to single po	int
reference d) Reduction of inductive loop area between power and return traces 10. Which among the below stated devices/equipments are preferred for elimination of ground and supply line noise especially in TTL/CMOS / ECL PCB designing a) Coupling capacitor	[] ion ?
b) Decoupling capacitor	
c) Snubber circuits	r 3
d) All of the above 11. Which among the below specified condition is precise in the crosstalk verifical mechanism using logic flow in opposite direction with the limit of avoiding dange interference in digital PCB designing?	ation erous
a) $Z_{\text{even}} > Z_{\text{odd}}$	
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$	
c) $Z_{\text{odd}} \geq 0.8 \ Z_{\text{even}}$ d) $Z_{\text{odd}} = Z_{\text{even}}$ 12. Which terminology of PCB represents a thin photo-sensitive polymer by supply photographic pattern of single traces or IC pads for etching? a) Prepreg	[] porting
b) Etching	
c) Photo-resist	r 1
d) Solder mask	[]



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13. Which problems are about to occur if PCB is not designed properly in a confir	ned
manner for digital circuits?	
A. Diffraction	
B. Refraction	
C. Ground & Supply-line Noise	r 7
D. Electromagnetic Interference	[]
a) A & B	
b) B & C	
c) C & D	
d) A, B, C, D	
14. Which among the following assists in obtaining the desired value of wave imp	pedance
in reflection phase while designing digital PCBs?	
A. Width of signal lines	
B. Distance between signal line and ground line	
C. Signal Delays	
D. Double Pulsing	
a) A & B	
b) B & C	
c) C & D	
d) A, B, C, D	[]
15. What should be the resistance of 0.6 mm wide conductor with 15 cm length a	nd 25
μm thickness of standard copper foil? (Assume $ρ = 1.7241 \times 10^{-6} (at 20^{\circ} C)$	
a) $118.2 \text{ m}\Omega$	
b) $138.2 \text{ m}\Omega$	
c) 172.4 m Ω	
d) 192.4 m Ω	
16. The actual cost of PCB can be evaluated on the basis of	
a) PCB size & material	
b) Number of layers	
c) Vias on PCB	
d) All of the above	[]
17. Which factors contribute to the occurrence of mechanical stress?	
a) Resonance	
b) Cracked Solder Joints	
c) Both a and b	
d) None of the above	[]
18. Which type of PCB requires minimum soldering on component side in order	to avoid
replacement oriented difficulties?	
a) Single-sided PCB	
b) Double-sided PCB	
c) Both a and b	
d) None of the above	[]

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- 19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?
- a) Increase in self-inductance
- b) Reduction in self-inductance
- c) Stability in self-inductance
- d) None of the above
- 20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

[]

- a)The use of a 3D component
- b) The use of a 3D component and component clearance rule
- c) The use of a courtyard
- d)The use of a courtyard and a component clearance rule

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ANSWERS

1. Answer: Convection

2. Answer: No holes or free electrons

3. Answer: Electrical Soldering

4. Answer: All of the above

5. Answer: Meniscus Rise Testing

6. Answer: Both a and b

7. Answer: Decrease in the distance between conductors

8. Answer: SON

. 9. Answer: Reduction of inductive loop area between power and return traces

10. Answer: Decoupling capacitor

11. Answer: Z_{odd} ≥ 0.8 Z_{even}

12. Answer: Photo-resist

13.Answer: C & D

14.Answer: A & B

15.Answer: 172.4 Mω

16. Answer: All of the above

17. Answer: Both a and b

18. Answer: Double-sided PCB

19. Answer: Reduction in self-inductance

20. Answer: The use of a courtyard and a component clearance rule

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Certificate Program on PCB Design Model Question Paper	
Branch/Sem: II ECE/I SEM Name of the Student: Vemula mounika RO	LL Number: 198BHA0U3U
1. Which phenomenon is not reduced by the circuit paths of low provided by power and return planes for shielding purposes? a) Radiation	est impedances especially
b) Convectionc) Noised) Crosstalk2. At absolute temperature, an intrinsic semiconductor has	ь V
a)A free electronsb) Many holesc) Many free electrons	
d) No holes or free electrons3. Which among the below stated soldering methods is also ren Resistance Soldering'?a) Iron Soldering	nowned as 'High Frequency
b) Furnace Solderingc) Torch Solderingd) Electrical Soldering4. Which among the below mentioned approaches belongs to the	id]
Testing? a) Impedance Testing b) Component Testing	
c) Apply Signal and check outputd) All of the above5. Which type of solderability testing is carried out for the gen due to immersion of wire or sheet metal specimen in a bath of	eration of solder sample molten solder?
a) Solder Bath Testingb) Meniscus Rise Testingc) Solder Iron Testingd) None of the above	ГЫ✓
6. What is/are the necessity/ies to provide guarding to precisiona) To increase leakage resistance b) To reduce capacitance between signal conductors & ground	n differential amplifiers?
c) Both a and b d) None of the above	[4]

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7. Which among the below mentioned assertions is not a way of cross-talk reduction			
while designing digital PCBs?			
a) Decrease in the distance between conductors			
b) Shielding of clock lines with guard strips			
c) Reduction in the loop area of circuits			1
d) Avoid running of parallel traces for longer distances especially for asynchronous		V	
signals[O]	nal	1	
8. Which among the below mentioned packages does not belong to the category of 'Sn	lai	1	
Outline Package'?			
a) SO			
b) SOP			
c) SOT	7		
d) SON]	1/	
9. Which among the below specified assertions is not a grounding consideration			
associated with ADC as well as DAC?			
a) Analog side to analog ground			
b) Digital side to digital ground			
c) Use of separate power supply and connection of their ground leads to single point			
reference			
d) Reduction of inductive loop area between power and return traces] ,	/	
10. Which among the below stated devices/equipments are preferred for elimination			
of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?			
a) Coupling capacitor			
b) Decoupling capacitor		Cart	
		1	
c) Snubber circuits d) All of the above)]	V	
11. Which among the below specified condition is precise in the crosstalk verification	1		
mechanism using logic flow in opposite direction with the limit of avoiding dangerou	S		
interference in digital PCB designing?			
a) $Z_{\text{even}} > Z_{\text{odd}}$			
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$			
c) $Z_{\text{odd}} \ge 0.8 Z_{\text{even}}$			
d) $Z_{\text{odd}} = Z_{\text{even}}$	2	1	/
12. Which terminology of PCB represents a thin photo-sensitive polymer by supporti	ng		
photographic pattern of single traces or IC pads for etching?			
a) Prepreg			/
b) Etching			/
c) Photo-resist		1	/
d) Solder mask	2]	V	
d) bolder mask			

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13. Which problems are about to occur if PCB is not designed properly in a confirmanner for digital circuits?	ied	
A. Diffraction		
B. Refraction		
C. Ground & Supply-line Noise		. /
D. Electromagnetic Interference	[C]	V
a) A & B		
b) B & C		
c) C & D		
d) A, B, C, D		
14. Which among the following assists in obtaining the desired value of wave imp	edanc	e
in reflection phase while designing digital PCBs?		
A. Width of signal lines		
B. Distance between signal line and ground line		
C. Signal Delays		
D. Double Pulsing		
a) A & B		
b) B & C		
c) C & D		. /
d) A, B, C, D	[a]	V
15. What should be the resistance of 0.6 mm wide conductor with 15 cm length a	nd 25	
μm thickness of standard copper foil? (Assume $ρ = 1.7241 \times 10^{-6} (at 20^{\circ} C)$		
a) 118.2 m Ω		
b) 138.2 mΩ		
c) 172.4 mΩ		. /
d) 192.4 mΩ	[C]	V
16. The actual cost of PCB can be evaluated on the basis of		
a) PCB size & material		
b) Number of layers		
c) Vias on PCB	e 15	
d) All of the above	[4]	V
17. Which factors contribute to the occurrence of mechanical stress?		
a) Resonance		
b) Cracked Solder Joints		
c) Both a and b	F - 7	1/
d) None of the above	[C]	
18. Which type of PCB requires minimum soldering on component side in order	to avo	1d
replacement oriented difficulties?		
a) Single-sided PCB		
b) Double-sided PCB		/
c) Both a and b	rl a	. /
d) None of the above	[b]	

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- 19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?
- a) Increase in self-inductance
- b) Reduction in self-inductance
- c) Stability in self-inductance
- d) None of the above

[C]

20. During post assembly testing, it was found that a latch on of the connectors cannot be fully extended due to other components located near by. What would have prevented the situation from occurring?

- a) The use of a 3D component
- b) The use of a 3D component and component clearance rule
- c) The use of a courtyard
- d)The use of a courtyard and a component clearance rule

[6]

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d) None of the above

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Department of Electronics and Communication Engineering

Certificate Program on PCB Design Model Question Paper

Branch/Sem: II ECE/I SEM Name of the Student: Devarampat: vistal: ROLL Number: 19	18BHAO412	
1. Which phenomenon is not reduced by the circuit paths of lowest impedances provided by power and return planes for shielding purposes? a) Radiation	especially	
b) Convection		
c) Noise		
d) Crosstalk	[b] L	/
2. At absolute temperature, an intrinsic semiconductor has		
a)A free electrons		
b) Many holes		
c) Many free electrons		/
d) No holes or free electrons	[d] V	
3. Which among the below stated soldering methods is also renowned as 'High	Frequency	
Resistance Soldering'?		
a) Iron Soldering		
b) Furnace Soldering		
c) Torch Soldering	c 12	,
d) Electrical Soldering	d) V	
4. Which among the below mentioned approaches belongs to the category of I	n-circuit	
Testing?		
a) Impedance Testing		
b) Component Testing		
c) Apply Signal and check output	[d] V	1
d) All of the above		
5. Which type of solderability testing is carried out for the generation of solde	r sample	
due to immersion of wire or sheet metal specimen in a bath of molten solder?		
a) Solder Bath Testing		
b) Meniscus Rise Testing		
c) Solder Iron Testing	[b] L	/
d) None of the above		
6. What is/are the necessity/ies to provide guarding to precision differential ar	upimers	
a) To increase leakage resistance		
b) To reduce capacitance between signal conductors & ground		
c) Both a and b	[c] \	/
d) None of the above		

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7. Which among the below mentioned assertions is not a way of cross-talk reduction while designing digital PCBs?			
a) Decrease in the distance between conductors			
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c) Reduction in the loop area of circuits			
d) Avoid running of parallel traces for longer distances especially for asynchronous	1		
signals[A]	1	1	
8. Which among the below mentioned packages does not belong to the category of 'S	mai		
Outline Package'?			
a) SO			
b) SOP			
c) SOT		. /	
-/	.]	V	
9. Which among the below specified assertions is not a grounding consideration			
associated with ADC as well as DAC?			
a) Analog side to analog ground			
b) Digital side to digital ground			
c) Use of separate power supply and connection of their ground leads to single point			
reference		1	
d) Reduction of inductive loop area between power and return traces		X	
10. Which among the below stated devices/equipments are preferred for elimination			
of ground and supply line noise especially in TTL/CMOS / ECL PCB designing?			
a) Coupling capacitor			
b) Decoupling capacitor			
c) Snubber circuits			
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11. Which among the below specified condition is precise in the crosstalk verification			
mechanism using logic flow in opposite direction with the limit of avoiding dangero			
interference in digital PCB designing?			
a) $Z_{\text{even}} > Z_{\text{odd}}$			
b) $Z_{\text{odd}} \ge 0.5 Z_{\text{even}}$			
c) $Z_{\text{odd}} \ge 0.3 Z_{\text{even}}$			
	Ы	V	
12. Which terminology of PCB represents a thin photo-sensitive polymer by support			
	an B		
photographic pattern of single traces or IC pads for etching?			
a) Prepreg			
b) Etching			
c) Photo-resist	ارس	. /	/
d) Solder mask	C]		

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C. Ground & Supply-line Noise D. Electromagnetic Interference a) A & B b) B & C c) C & D d) A, B, C, D 14. Which among the following assists in obtaining the desired value of wave impedance in reflection phase while designing digital PCBs? A. Width of signal lines B. Distance between signal line and ground line C. Signal Delays D. Double Pulsing a) A & B b) B & C c) C & D d) A, B, C, D 15. What should be the resistance of 0.6 mm wide conductor with 15 cm length and 25 μ m thickness of standard copper foil? (Assume $\rho = 1.7241 \times 10^{-6} (at \ 20^{\circ} \ C)$ a) 118.2 m Ω b) 138.2 m Ω c) 172.4 m Ω d) 192.4 m Ω d) 192.4 m Ω 16. The actual cost of PCB can be evaluated on the basis of	13. Which problems are about to occur if PCB is not designed properly in a confirmanner for digital circuits?A. DiffractionB. Refraction	ned	
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a) Resonance b) Cracked Solder Joints c) Both a and b d) None of the above 18. Which type of PCB requires minimum soldering on component side in order to avoid		[d]	/
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d) None of the above [6] 18. Which type of PCB requires minimum soldering on component side in order to avoid			
18. Which type of PCB requires minimum soldering on component side in order to avoid		[6]	1
	18 Which type of PCB requires minimum soldering on component side in order		id
a) Single-sided PCB			
b) Double-sided PCB			1
c) Both a and b		r/ 1	/
d) None of the above	d) None of the above		

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- 19. What effects can be observed if the separate power and ground planes are provided with large conducting surfaces for better decoupling in PCB layouts?
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- b) The use of a 3D component and component clearance rule
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- d)The use of a courtyard and a component clearance rule

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[b]1.







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Certificate Program on PCB Design Assessment Marks

A.Y: 2020-2021

Year: II

S. No	Reg. No	Name of the Candidate	Marks
1	198B1A0401	APPALA DURGA MAHALAKSHMI	19
2	198B1A0402	BANDARU DHARANI	17
3	198B1A0404	BOGALA CHINNAKKA	18
4	198B1A0405	CHALLA THRIVENI	17
5	198B1A0407	CHANDRA UMARANI	18
6	198B1A0408	CHEMBETI VASANTHI	19
7	198B1A0410	DANDIBOYINA SRAVANI	18
8	198B1A0411	DEVARAKONDA NEERAJA	18
9	198B1A0412	DEVARAMPATI VISHALI	18
10	198B1A0413	DEVATHA NAGAJYOTHI	19
11	198B1A0414	DUDDIKUNTA JYOTHI REDDY	18
12	198B1A0415	DUMPA SANDHYA	19
13	198B1A0416	EEMANI SWAPNA	19
14	198B1A0417	JAMPANI HARI VANDANA	20
15	198B1A0418	JYOSHNA VAKA	16
16	198B1A0419	KONDURI SANTHOSHI POORNIMA	19
17	198B1A0420	KOTA YAMINI	18
18	198B1A0421	MADIREDDY ANUSHA	19
19	198B1A0422	MANDAPATI SAI PREETHI	17
20	198B1A0424	PADARTHI VENKATA SAI AKHILA	19
21	198B1A0425	PARIMI SUREKHA	16
22	198B1A0426	PATHURI ABHINAYA	18
23	198B1A0427	PUNUGOTI BHULAKSHMI	18
24	198B1A0428	RAVURI LAKSHMI	18
25	198B1A0429	SHAIK HUZURUNNISA	15
26	198B1A0430	SHAIK RUKHYA	19
27	198B1A0431	TAMALAPAKULA KAVITHA RANI	18
28	198B1A0432	THATI THOTI PARIMALA	19
29	198B1A0433	VADLAMUDI DEEPTHI	17
30	198B1A0434	VEMULA MOUNIKA	19
31	198B1A0436	ANUMOLU MANIDEEP	16
32	198B1A0437	BELLAMKONDA DANAMURTHI	16
33	198B1A0439	CHITIRALA VISHNU VARDHAN	16
34	198B1A0440	DEPURI HARIKRISHNA	17





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S. No	Reg. No	Name of the Candidate	Marks
35	198B1A0441	EDAMAKANTI RAVI	18
36	198B1A0442	GONUGUNTA HARI BABU	16
37	198B1A0443	GONUGUNTA MAHESH	19
38	198B1A0444	KANDLAGUNTA NAVEEN KUMAR	18
39	198B1A0445	KASU DURGA RAJESWAR REDDY	19
40	198B1A0446	KATIKALA AMITH	18
41	198B1A0447	KESAMREDDY PRABHAKAR	17
42	198B1A0448	KUNCHALA ASHOK	18
43	198B1A0449	KUNCHALA HARESH	17
44	198B1A0450	MADALA AMARNADH	18
45	198B1A0451	MADDULURI SIVA SAI KUMAR	19
46	198B1A0452	MAMILLAPALLI SUMANTH KUMAR	18
47	198B1A0453	MANNEM MAHESH	18
48	198B1A0454	MEDIKONDA RAMAKRISHNA	17
49	198B1A0455	MOLABANTI NAGA SRINU	19
50	198B1A0456	MUNAGALA CHARAN REDDY	20
51	198B1A0457	PAMBA ANJAIAH	20
52	198B1A0458	RAVULAPALLI CHARAN KUMAR	16
53	198B1A0459	RENUMALA NAGAMUTTHU	19
54	198B1A0460	SHAIK AZMAL	16
55	198B1A0461	SHAIK SHAJAHAN	20
56	198B1A0462	TELUKUTLA GOPI	16
57	198B1A0463	THANNIRU DURGA MALLESHWAR	19
58	198B1A0464	VADDEMPUDI REVANTH	18
59	198B1A0465	PULI JAYARAMIREDDY	19
60	208B5A0401	KUNCHALA AKHILA	18
61	208B5A0402	POTU SRI MOUNIKA	17
62	208B5A0403	SYED TASNIMKAUSAR	17
63	208B5A0404	VENNAPUSA ESWAR REDDY	17
64	208B5A0405	SYED JAFAR	19
65	208B5A0406	TANNIRU MANOJ KUMAR	16

Cordinator

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HEAD OF THE DEPARTMENT,

HEAD OF THE DEPARTMENT,

Department of E.C.E.

RISE Krishna Sai Gandhi Group

RISE Krishna Sai Gandhi Group

Of Inc. Hullong, Valluru, A.P. 523 272

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RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS: ONGOLE DEPARTMENT OF ECE

Certificate program on PCB Design 22-03-2021 to 26-03-2021

The Certificate Program conducted by ECE department on 22nd - 26th March 2021 in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS in association with Center for Electronics System Design (CESD)

Department of Electronics & Communication Engineering

RISE KRISHNA SAI GAND

Objectives of conducting Certificate program

- To make students learn and interact with renowned industry experts.
- Make Students to receive an unparallel education on the art of PCB Designing Certificate program with personal one on one attention.
- To make every student an expert in designing their own PCB board which would be very useful for developing their own projects.

Overview about Certificate Program:

The aim of this **Certificate Program** is to make the students learn the designing and manufacturing of a printed circuit board using open source KICAD PCB design software and with various active and passive components such as Regulators, Diodes, Resistors, Capacitors, Inductors, Switches, e.t.c.

Technical Support:

The Certificate Program was conducted in collaboration with Center for Electronics System Design (CESD) from Vijayawada. The company has a fast growth in PCB designing. The company's director Mr. Finney Daniel accompanied with Seven Trainers attended the Certificate Program for guiding the students in learning the technologies of the PCB Design Certificate Program. They have taken about 32 hours of theoretical and practical sessions.

Department of ECE:

Department of ECE has taken the opportunity to conduct the in RISE KRISHNA SAI GANDHI GROUP OF INSTITUTIONS. As the theme of the Certificate Program is the core for the department, it's a nice opportunity for the students to learn the technology and to implement that practically.

Technical Report on Certificate Program:

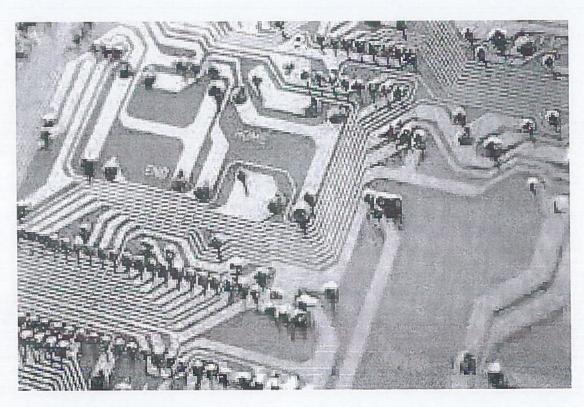
The Technical team of Center for Electronics System Design (CESD) has described the entire designing process in a step by step procedure.

1. Basic PCB Concepts

First of all they have given the concepts which will be very helpful for designing the PCB practically, using some power point presentations. In this theoretical explanation part they have explained about the KI-CAD software and the use of software for further practical implementation in designing the PCB. They have also

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given a briefing about active and passive electronic components which they will be using in a PCB.



2. Editing and Routing

Editing and Routing is the basic step and it is one of the important step for designing a PCB. Editing and Routing gives the circuit layout from one component to the other components. Soldering plays a key role in this step.





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3. Creation of Library and Components & Report Generation

This is a step done using KI-CAD tools. In this step the components in the circuit and the respective libraries are selected in this software. So that the required circuit will be designed in the software and a print of the same will be taken on a sheet. The same print will be useful for the further process.

4. Toner Transfer Method

This is the step where the designed circuit will be pasted on the wafer and this will be passed through a temperature of about 160 to 180 degrees so that the tracks of the circuit will be remained on the wafer. The tracks will be a conductive type.

5. Drilling Technique

The board will be drilled with holes where the components have to be placed; the holes will be drilled in the board depending on the terminals available for the components in the design. The hole should be in the size so that the terminal has to be freely placed in the hole.

6. Soldering Technique

The components that are placed in the board should be soldered to the track so that the circuit is connected as per the design. After this step the engraved PCB will be ready to use.

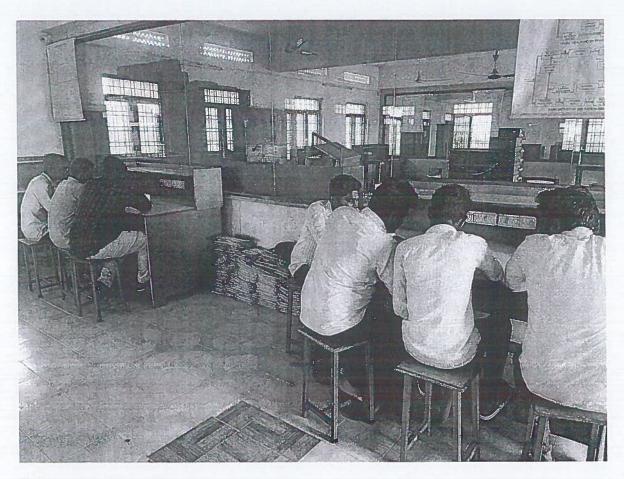
The Department conducted test on PCB Design for Electronic components and all project models are exhibited in the respected department

Student Response

Almost 65 students had taken part in the Certificate Program. All the students responded that they have learned and had hands on experience in designing a PCB. They are very excited in participation in this Certificate Programand requested for more Certificate Program in similar way so that they can simultaneously gain the practical knowledge.

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Distribution of Certificates

At the last day question answer session and certificate distribution function started on 4:30 PM. Feedbacks regarding workshop are provided by various students.

All the students were awarded with a participation certificate from the company Center for Electronics System Design(CESD). Principal Dr.K.V.Subrahmanyam garu awarded the certificates to all the students by hand. He personally congratulated every student for participating in the event and making it successful.

Vote of Thanks

Mr.S V Ravi Kumar beloved HOD of ECE Department thanked every student for their active participation and interest in participating in the Certificate Program and mentioned about the activities conducted in the college by the department. He promised that department will continue its assistance in conducting these sorts of Certificate Programs and seminars in future.



RISE KRISHMA SAI GANDHI GROUP OF INSTITUTIONS VALLURU: ONGCAE. He thanked the technical support given by **Center for Electronics System Design (CESD).** He personally felt very happy for the response of the company and satisfied with the way they conducted the Certificate Program.

He mentioned about the marvelous support given by the Principal Dr.K.V.Subrahmanyam garu to the department in conducting these Certificate Program. He also thanked for the personal interest taken by him in encouraging the department in all aspects.

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Date: 26-03-2021.

CLOSING REPORT

To, The Principal, RISE Krishna Sai Gandhi Group of Institutions.

As per the approved schedule, the ECE department has conducted a Certificate Program on "PCB Design" at ECE Seminar hall from 22-03-2021 to 26-03-2021. 65 students of II ECE have participated in this program. Sri F.Daniel, Director, Center for Electronics Systems Design (CESD), Vijayawada, AP, acted as the resource person for this program.

Main issues addressed:

- 1. Basic PCB Concepts
- 2. Editing and Routing
- 3. Creation of Library and Components & Report Generation
- 4. Toner Transfer Method
- 5. Drilling Technique
- 6. Soldering Technique

We are expecting your support in future also. Thanking you sir,

Yours faithfully,

HEAD OF THE DEPARTMENT Department of E.C.F. Financial Sai Gandhi Group c' METAHORE A.P. 523 272

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